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ENABLING ARTIFICIAL INTELLIGENCE WITH ENGINEERED SUBSTRATES

January 2026

DISCLAIMER

This document is provided by Soitec (the "**Company**") for information purposes only. The Company's business operations and financial position are described in the Company's 2024-2025 Universal Registration Document (which notably includes the Annual Financial Report) and the Company's 2025-2026 Half-Year Report.

The 2024-2025 Universal Registration Document was filed with the French stock market authority (Autorité des Marchés Financiers, or AMF) on June 11, 2025 and the 2025-2026 Half-Year Report on November 29, 2025. The French version of the 2024-2025 Universal Registration Document and the 2025-2026 Half-Year Report, together with English courtesy translation for information purposes, is available for consultation on the Company's website (www.soitec.com), in the section Investors - Regulated Information - Financial reports and results & other regulated releases.
Your attention is drawn to the risk factors described in Chapter 2.1 (Risk factors and controls mechanism) of the 2024-2025 Company's Universal Registration Document.

This document contains summary information and should be read in conjunction with the 2024-2025 Universal Registration Document and the 2025-2026 Half-Year Report.

This document contains certain forward-looking statements. These forward-looking statements relate to the Company's future prospects, developments and strategy and are based on analyses of earnings forecasts and estimates of amounts not yet determinable. By their nature, forward-looking statements are subject to a variety of risks and uncertainties as they relate to future events and are dependent on circumstances that may or may not materialize in the future. Forward- looking statements are not a guarantee of the Company's future performance. The occurrence of any of the risks described in Chapter 2.1 (Risk factors and controls mechanism) of the 2024-2025 Universal Registration Document may have an impact on these forward- looking statements. In particular, ongoing geopolitical tensions as well as persistent inflationary pressures, monetary policy and exchange rates uncertainty, and supply chain disruptions, may have consequences that are more significant or longer-lasting than currently anticipated in these forward- looking statements.

Any market shares presented herein are based on internal estimates and relate to that share of the market segment served and addressed by Soitec which may exclude broader segments of the market and competing technologies.

The Company's actual financial position, results and cash flows, as well as the trends in the sector in which the Company operates may differ materially from those contained in this document. Furthermore, even if the Company's financial position, results, cash-flows and the developments in the sector in which the Company operates were to conform to the forward- looking statements contained in this document, such elements cannot be construed as a reliable indication of the Company's future results or developments.
The Company does not undertake any obligation to update or make any correction to any forward-looking statement in order to reflect an event or circumstance that may occur after the date of this document.

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Notably, this document does not constitute an offer or solicitation to purchase, subscribe for or to sell securities in the United States. Securities may not be offered or sold in the United States absent registration or an exemption from the registration under the U.S. Securities Act of 1933, as amended (the "**Securities Act**"). The Company's shares have not been and will not be registered under the Securities Act. Neither the Company nor any other person intends to conduct a public offering of the Company's securities in the United States.
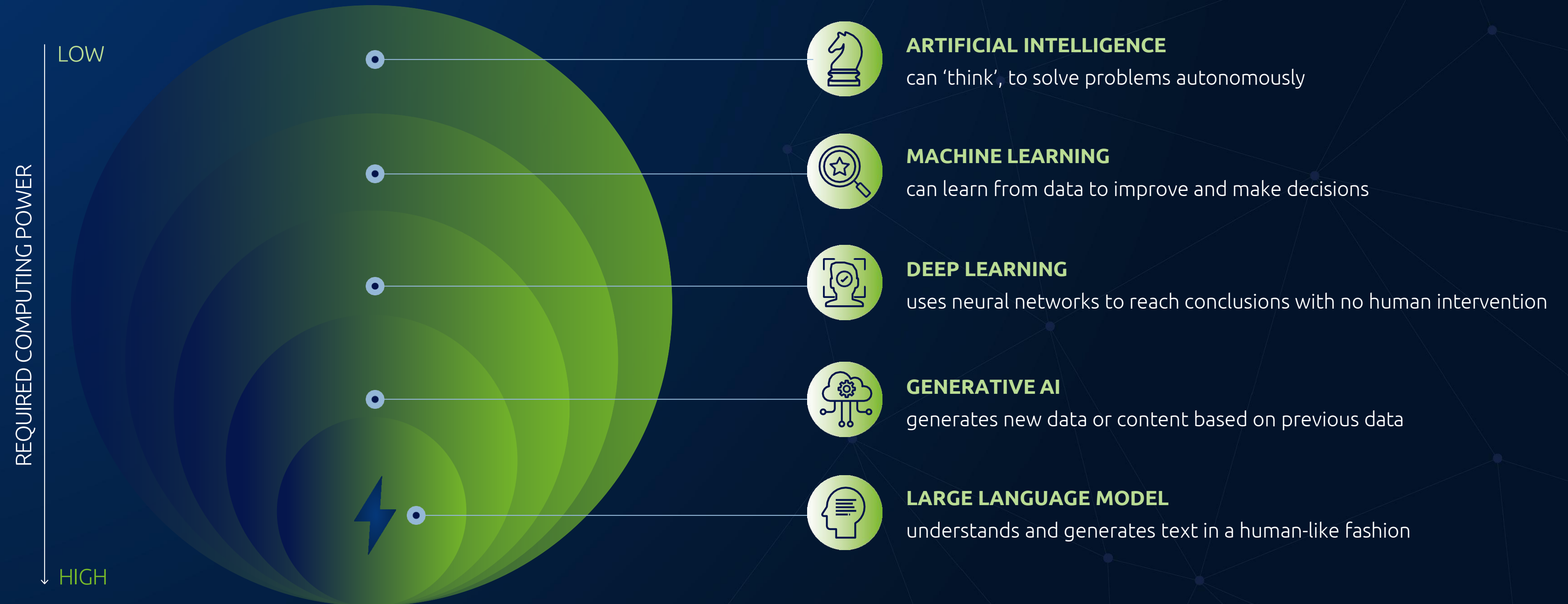
AGENDA

#01

AI FUNDAMENTALS

#02

ENGINEERED SUBSTRATES
FOR CLOUD AI
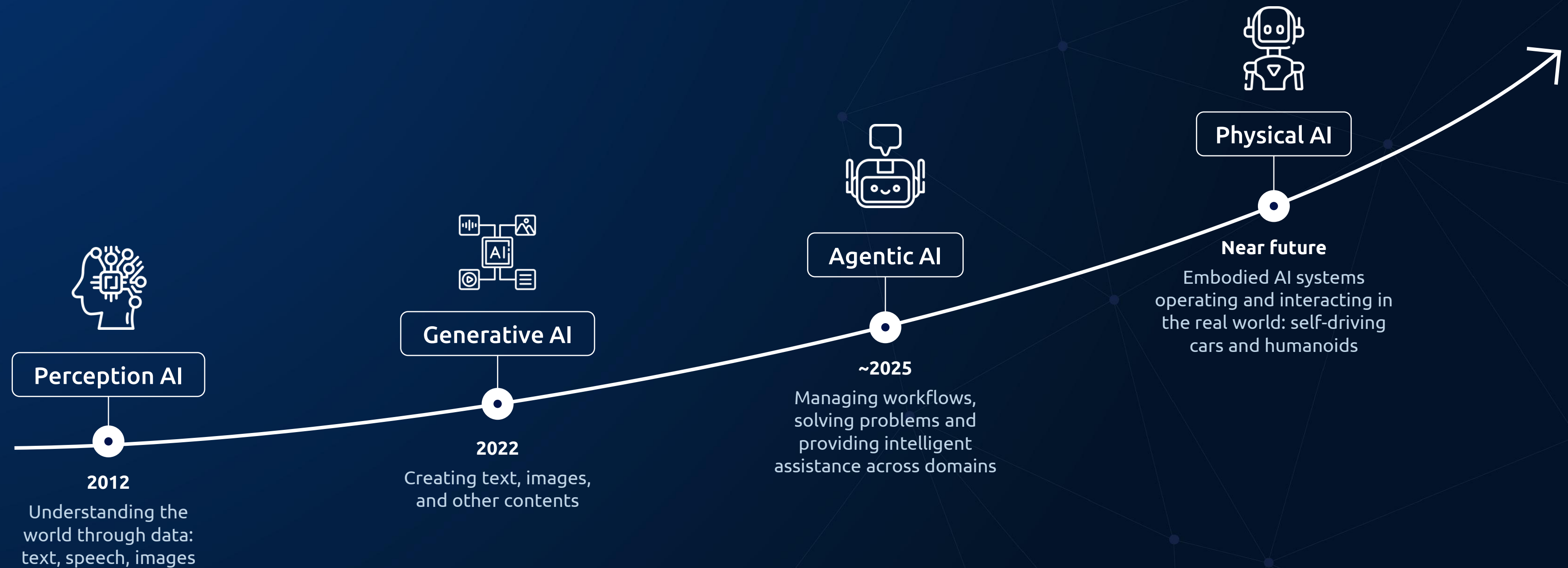
#03

ENGINEERED SUBSTRATES
FOR EDGE AI

01
AI
FUNDAMENTALS

WHAT IS ARTIFICIAL INTELLIGENCE?

LOW

REQUIRED COMPUTING POWER

HIGH

ARTIFICIAL INTELLIGENCE
can 'think', to solve problems autonomously

MACHINE LEARNING
can learn from data to improve and make decisions

DEEP LEARNING
uses neural networks to reach conclusions with no human intervention

GENERATIVE AI
generates new data or content based on previous data

LARGE LANGUAGE MODEL
understands and generates text in a human-like fashion

Source: Accenture, SCS

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ADVANCING TOWARD PHYSICAL AI: THE NEXT FRONTIER OF AI

Perception AI

2012
Understanding the world through data: text, speech, images

Generative AI

2022
Creating text, images, and other contents

Agentic AI

~2025
Managing workflows, solving problems and providing intelligent assistance across domains

Physical AI

Near future
Embodied AI systems operating and interacting in the real world: self-driving cars and humanoids

CHALLENGES FROM THE APPLICATIONS TO THE HARDWARE LAYERS
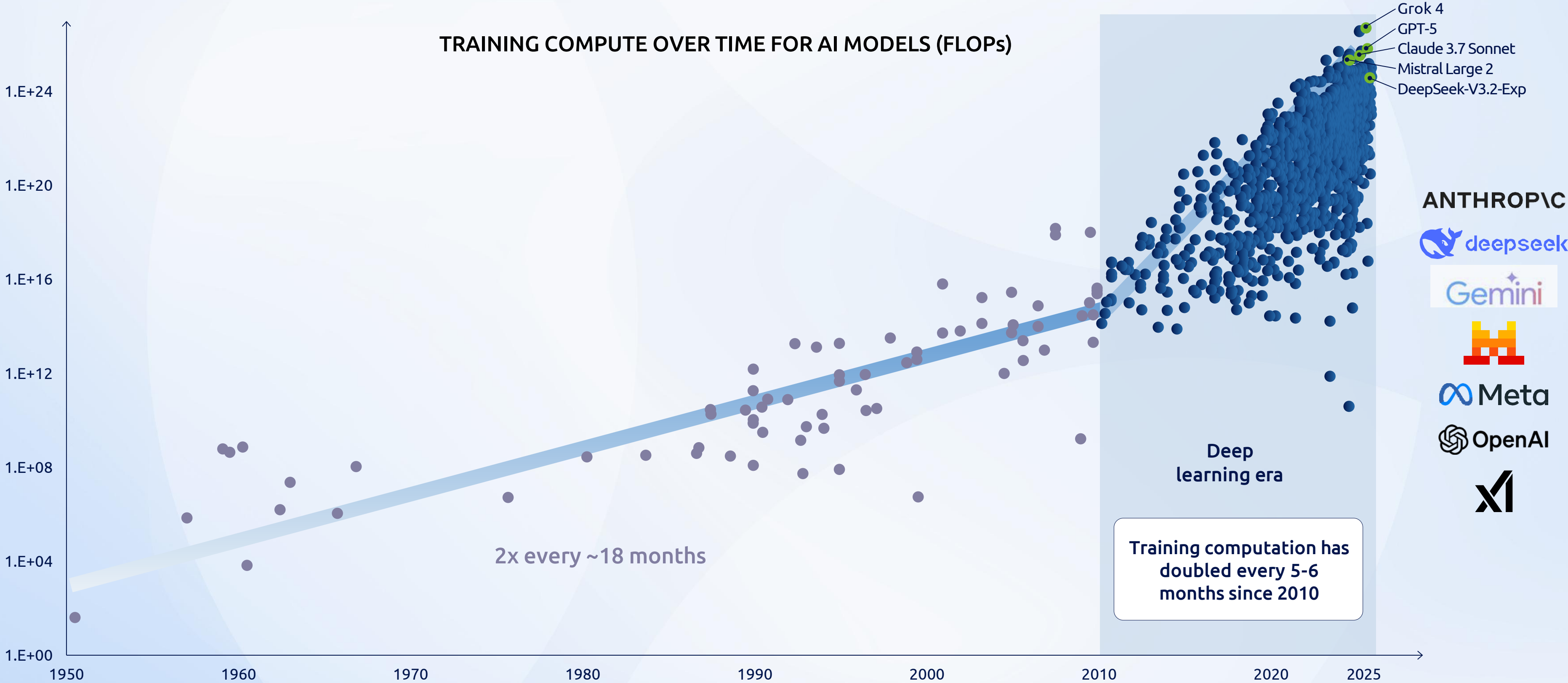## SOITEC TECHNOLOGY TO LEVERAGE CLOUD AI & EDGE AI NEW CHALLENGES

APPLICATIONS LAYER

Architecture & Infrastructure	Smart assistants	Image generation	ADAS/AD	Smart City	Voice recognition	Face recognition	Real-time sound processing	Industry 4.0

MODEL LAYER

Large Language Models

General purpose LLM and other models (such as ChatGPT, DALL-E…) replicating human-like thinking and decision-making processes

Domain-Specific Models

AI models trained on specific data to perform tasks with greater precision (enterprise, professional content creation, simulated data, etc.)

HARDWARE LAYER

AI data center infrastructure

Hyperscale data centers and enterprise servers powered by AI accelerators running large models for highly complex tasks

On-device Edge AI

Edge AI chips running optimized AI models at low power for lower complexity tasks

Source: Qualcomm, Red Hat

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AI MODEL COMPLEXITY GROWING EXPONENTIALLY
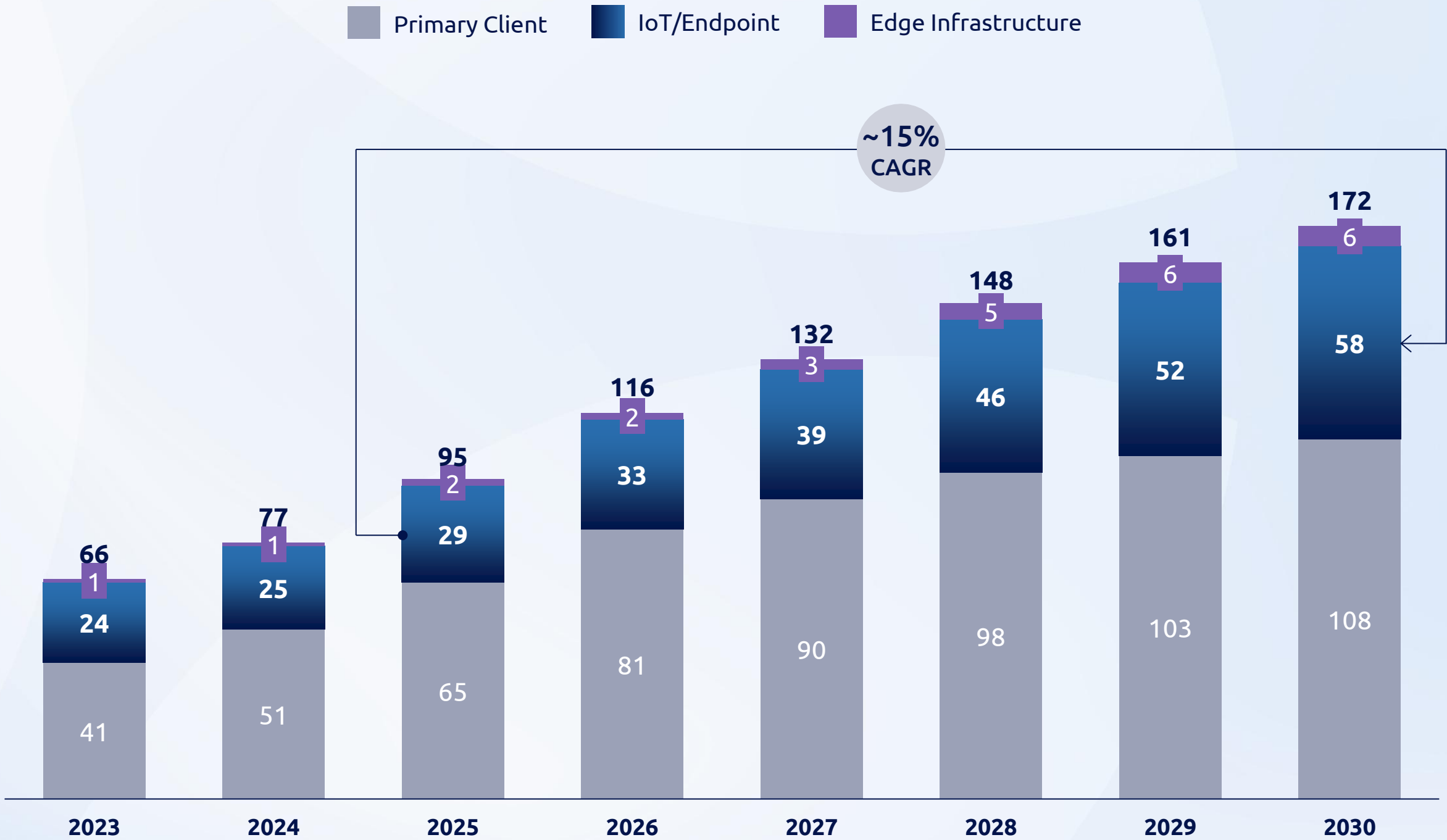## DRIVING AN UNPRECEDENTED SURGE IN COMPUTING POWER DEMAND

TRAINING COMPUTE OVER TIME FOR AI MODELS (FLOPs)

Grok 4
GPT-5
Claude 3.7 Sonnet
Mistral Large 2
DeepSeek-V3.2-Exp

ANTHROP\C
deepseek
Gemini
Meta
OpenAI
xAI

2x every ~18 months

Deep
learning era

Training computation has doubled every 5-6 months since 2010

1.E+24
1.E+20
1.E+16
1.E+12
1.E+08
1.E+04
1.E+00

1950   1960   1970   1980   1990   2000   2010   2020 2025

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FROM CLOUD AI TO EDGE AI
LOWER LATENCY, HIGHER ENERGY EFFICIENCY, AND PRIVACY BY DESIGN

FUTURE
ADDING ON-DEVICE COMPUTING

IN-MEMORY COMPUTE AT THE EDGE WITH HIGH EFFICIENCY INFERENCE

NOW
ADDING EDGE COMPUTING

AI TRAINING IN THE CLOUD INFERENCE AT THE EDGE

BEFORE
CLOUD COMPUTING ONLY

AI TRAINING IN THE CLOUD INFERENCE IN THE CLOUD

EDGE AI SILICON REVENUE FORECAST BY MARKET SEGMENT ($B)

Legend: Primary Client | IoT/Endpoint | Edge Infrastructure

~15% CAGR

Year	Primary Client	IoT/Endpoint	Edge Infrastructure	Total
2023	41	24	1	66
2024	51	25	1	77
2025	65	29	2	95
2026	81	33	2	116
2027	90	39	3	132
2028	98	46	5	148
2029	103	52	6	161
2030	108	58	6	172

Source: IDC Embedded and Intelligent Systems, Semi AI Module 2025

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ENGINEERED SUBSTRATES FOR CLOUD AI

AI-LED SURGE IN DATA CENTER CAPACITY DEMAND THROUGH 2030
PLACING INCREASING STRAIN ON INFRASTRUCTURE: BANDWIDTH, POWER, AND ENERGY EFFICIENCY

GLOBAL AI DATACENTER CAPITAL SPENDING (IN $B)

- Microsoft
- Meta
- Amazon
- Google
- Oracle
- Alibaba
- CoreWeave
- Others

>20% CAGR

~250 (2024)
~400 (2025E)
~830 (2030E)

2022 · 2023 · 2024 · 2025E · 2026E · 2027E · 2028E · 2029E · 2030E
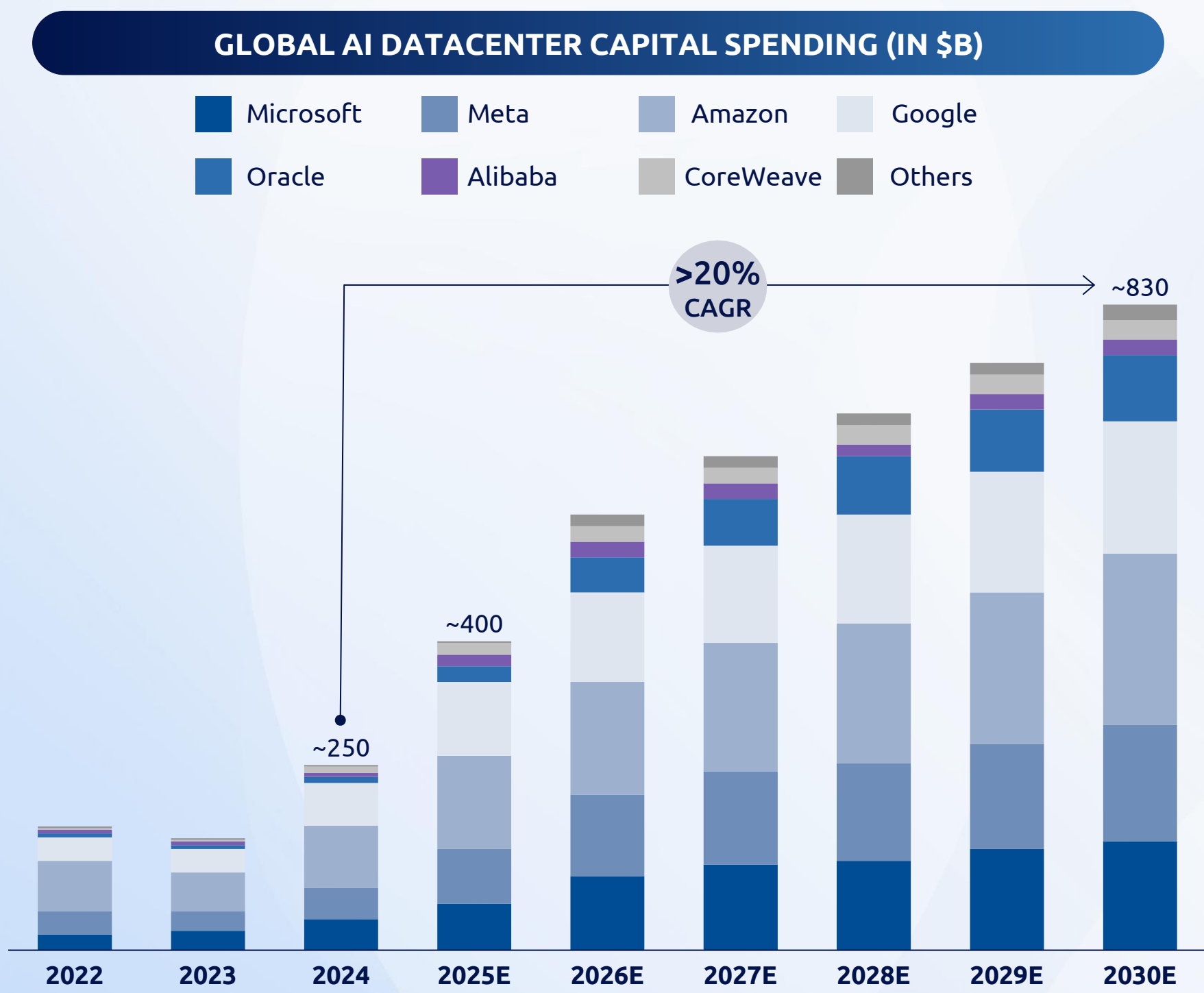
Source: BNP Paribas Research, Soitec estimates

ESTIMATED GLOBAL CAPACITY DEMAND (IN GW)

- AI Servers
- General-Purpose Servers

>20% CAGR

~x3.5

Year	AI Servers	General-Purpose Servers	Total
2025E	44	38	82
2026E	62	40	103
2027E	83	45	128
2028E	102	50	153
2029E	124	56	181
2030E	156	64	219
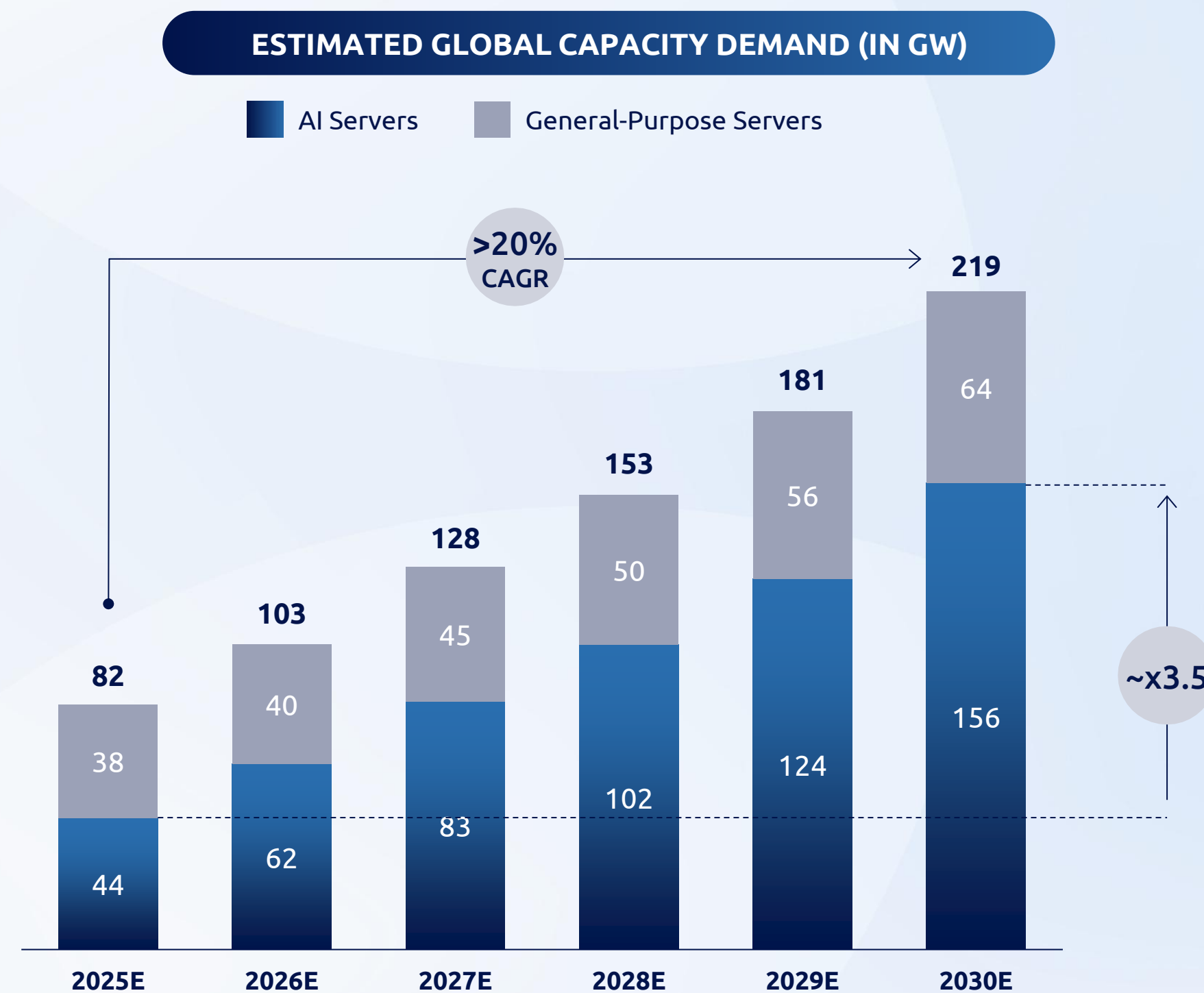
Source: McKinsey, August 2025

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AI DATA CENTERS ARE SCALING ACROSS, OUT, UP, AND IN

PERVASIVE OPTICAL INTERCONNECTS ARE ESSENTIAL TO OVERCOME THE BANDWIDTH BOTTLENECK

SCALE ACROSS	SCALE OUT	SCALE UP	SCALE IN

SCALE ACROSS

DC#2

DC#3

DC#1

Across datacenters
(10s to 100s km range)

Pluggable Optics

Coherent-lite

SHIPPING NOW

SCALE OUT

10k – 100k+ chips

Across racks
(10s meters to a few km range)

**Pluggable Optics
or CPO gen 1.0**

SHIPPING NOW

SCALE UP

100s of chips

Within a rack
(1-10 meters range)

CPO gen 2.0

(aka Optical I/O)

2027-2028 (estimated)

SCALE IN

10s of chiplets
in a single package

Within a package
(1 to 10s mm range)

CPO gen 3.0

(aka Photonics Interposer)

>2030 (estimated)

Optical connectivity

Copper connectivity

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OPTICAL INTERCONNECTS TO SUPPORT THE NEXT SCALE OF AI DATA CENTERS
FROM PLUGGABLE INTERCONNECTS TO CO-PACKAGED OPTICS

FROM ELECTRONS TO PHOTONS – THE SHIFT POWERING THE AI ERA

Distance

- Data Center Interconnect (DCI)
- Rack-to-Rack
- Board-to-Board
- Chip-to-Module
- Chip-to-Chip

using **PHOTONS**
Lightspeed
Limited losses
Bandwidth 10,000 x greater

OPTICAL

ELECTRICAL

Operating window today
Operating window within a decade

Data rate

using **ELECTRONS**
Fast
Lossy
Limited bandwidth

OPTICAL INTERCONNECTS – FROM PLUGGABLES TO CPOs

HIGHER BANDWIDTH / LOWER POWER

TOP VIEW   **CROSS VIEW**

OPTICAL I/O

CO-PACKAGED OPTICS

ON-BOARD OPTICS
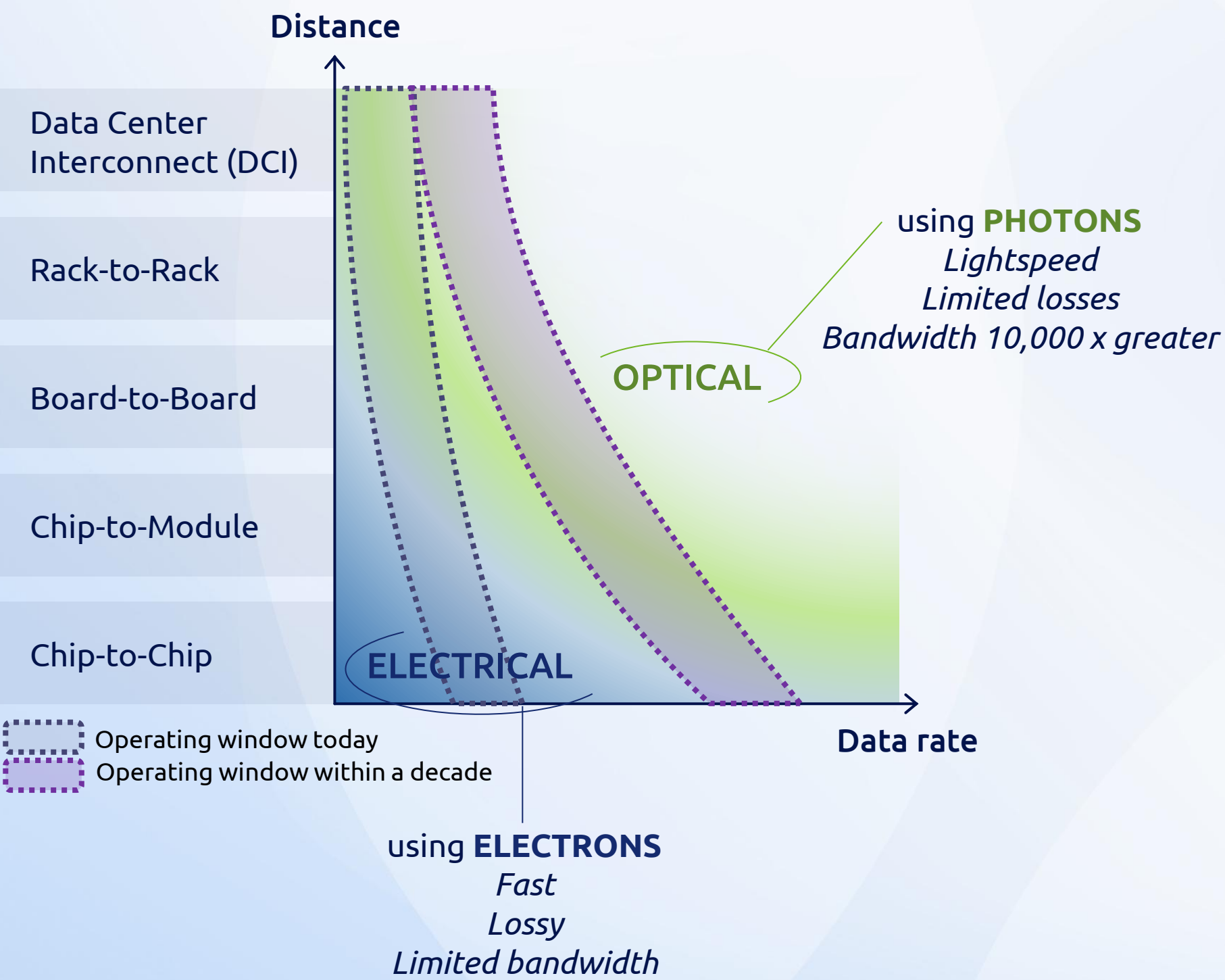
PLUGGABLE OPTICS
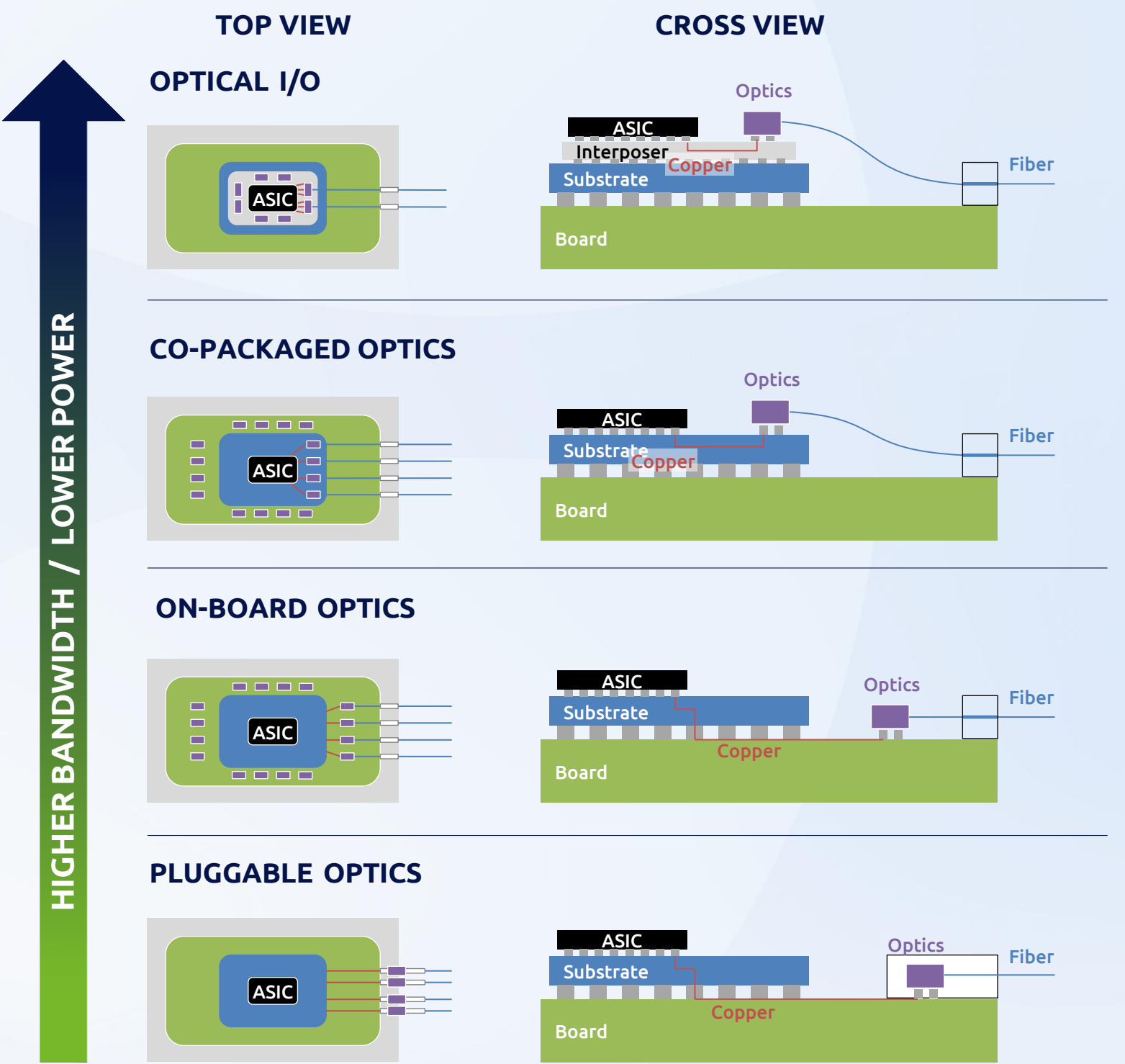
OPTICAL INTERCONNECTS DEMAND SOARS
INCREASING HIGH BANDWIDTH CONNECTIVITY IN DATA CENTERS DRIVING HIGHER SEMICONDUCTOR CONTENT GROWTH

OPTICAL INTERCONNECTS SALES SOARS AS AI DEMAND INTENSIFIES
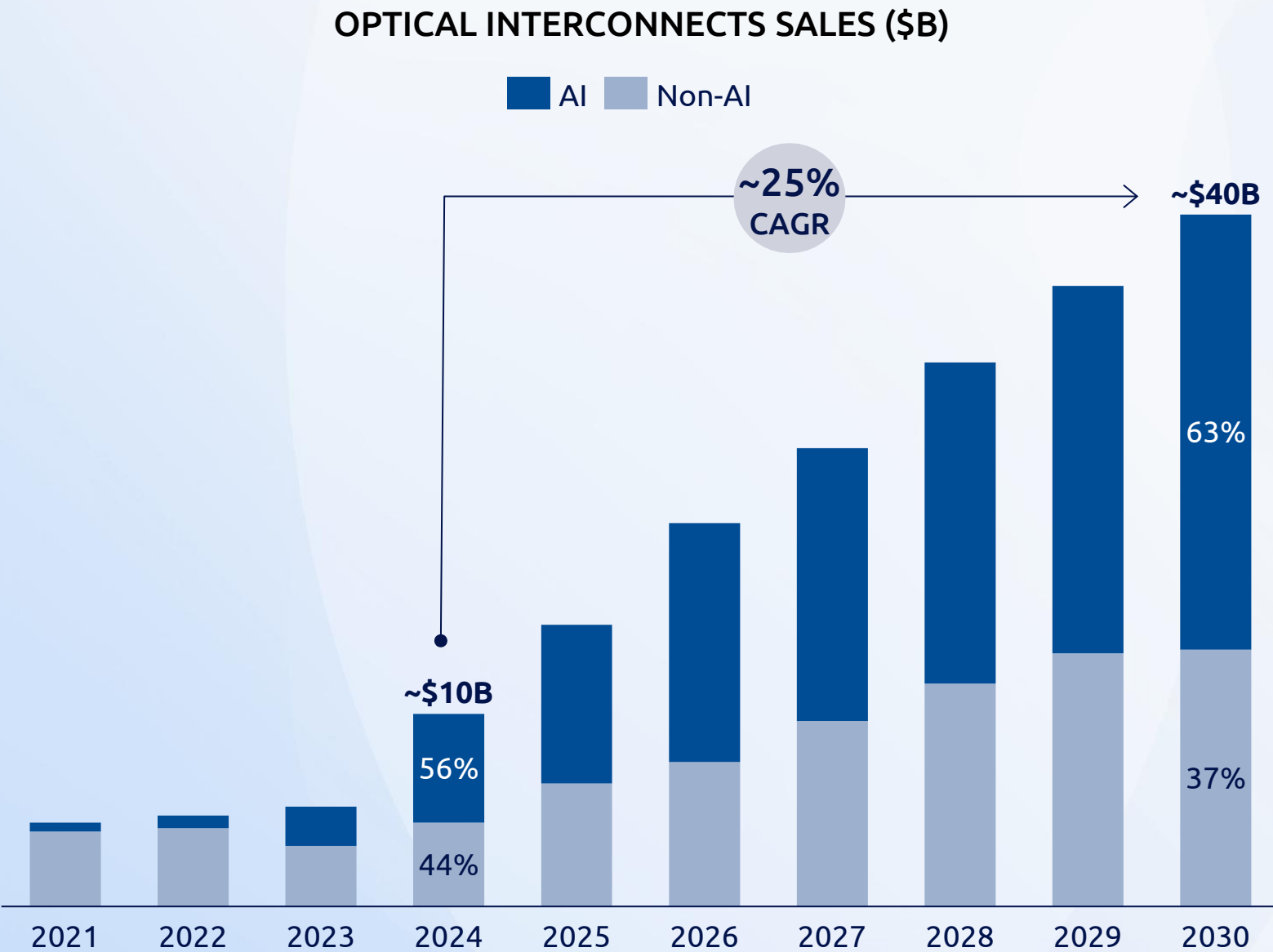
OPTICAL INTERCONNECTS GROWING FASTER THAN XPUs

OPTICAL INTERCONNECTS SALES ($B)

■ AI ■ Non-AI

~25% CAGR

~$40B

~$10B

Year	
2024 AI	56%
2024 Non-AI	44%
2030 AI	63%
2030 Non-AI	37%

2021 2022 2023 2024 2025 2026 2027 2028 2029 2030

128 Interconnects — 128 XPUs

2k Interconnects — 1k XPUs

75k Interconnects — 25k XPUs

10M Interconnects — 1M XPUs
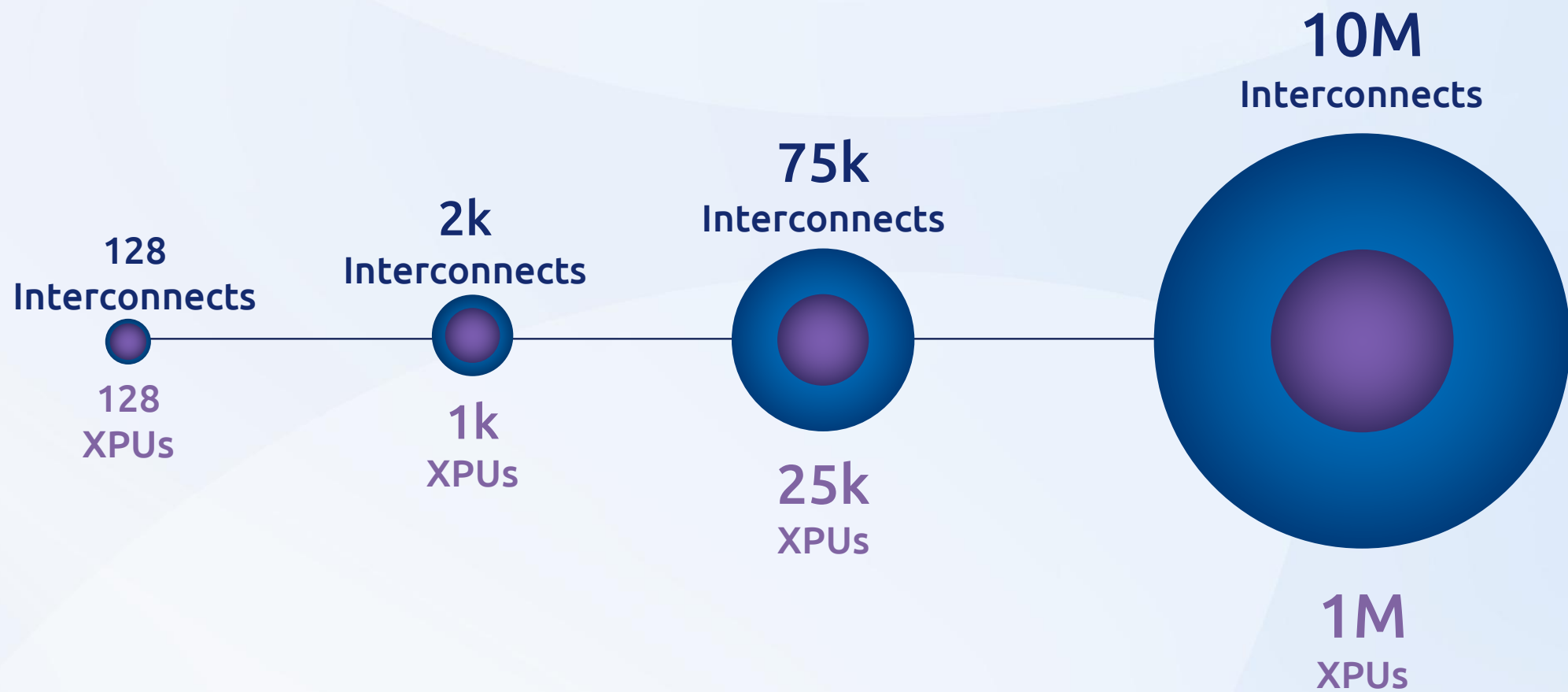
Source: Marvell investor presentation (2024), LightCounting

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OPTICAL INTERCONNECTS SHIFTING TO HIGHER DATA RATES

SILICON PHOTONICS & LNOI – TWO TECHNOLOGIES ADDRESSING DIFFERENT SEGMENTS

SHIFT TOWARD HIGHER-SPEED TRANSCEIVERS

To accommodate increasing demand in data transmission

ETHERNET TRANSCEIVER MARKET BY DATA RATE ($B)

Legend:
- 100G
- 200G
- 400G
- 800G
- 1.6T
- 3.2T
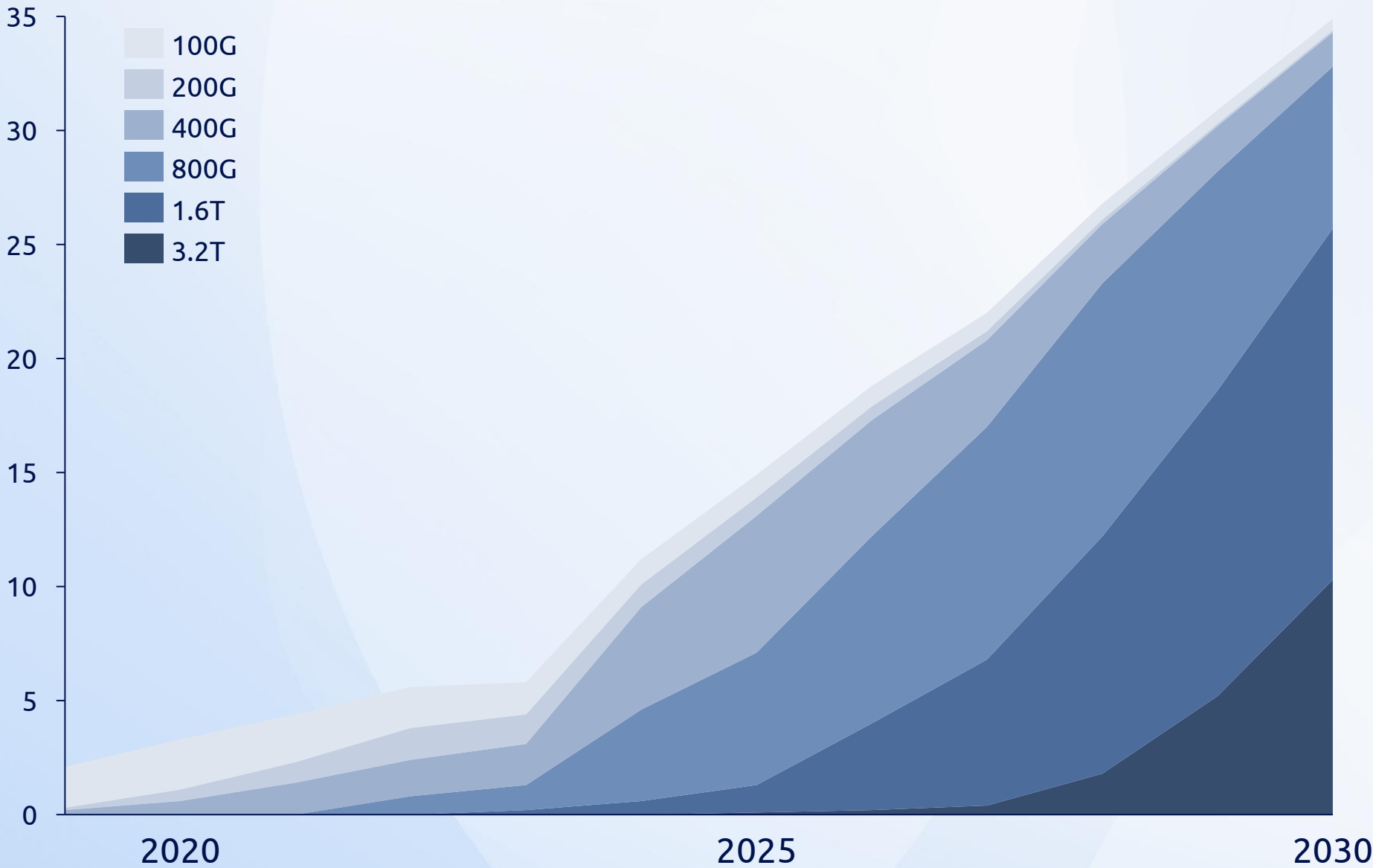
Source: LightCounting

SILICON PHOTONICS EMERGES AS THE DOMINANT MODULATOR PLATFORM

Driven by scalability, cost, and integration advantages
LNOI to complement Silicon Photonics (<1.6T), addressing the 1.6T-3.2T data rate
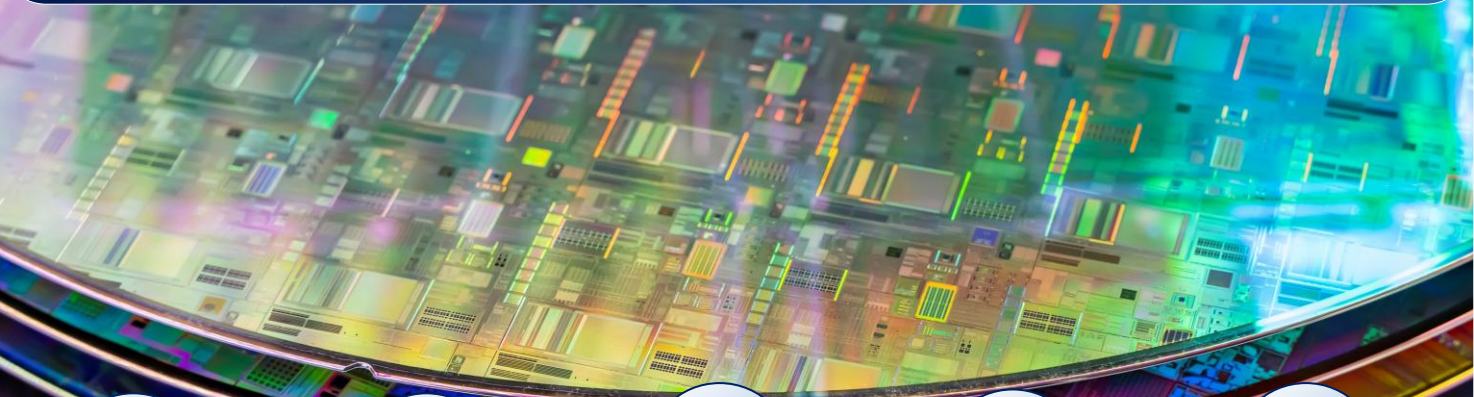
TRANSCEIVER MARKET BY MODULATOR TECHNOLOGY ($B)

Legend:
- TFLN/LNOI & others
- GaAs
- InP
- **Silicon Photonics**

>x3
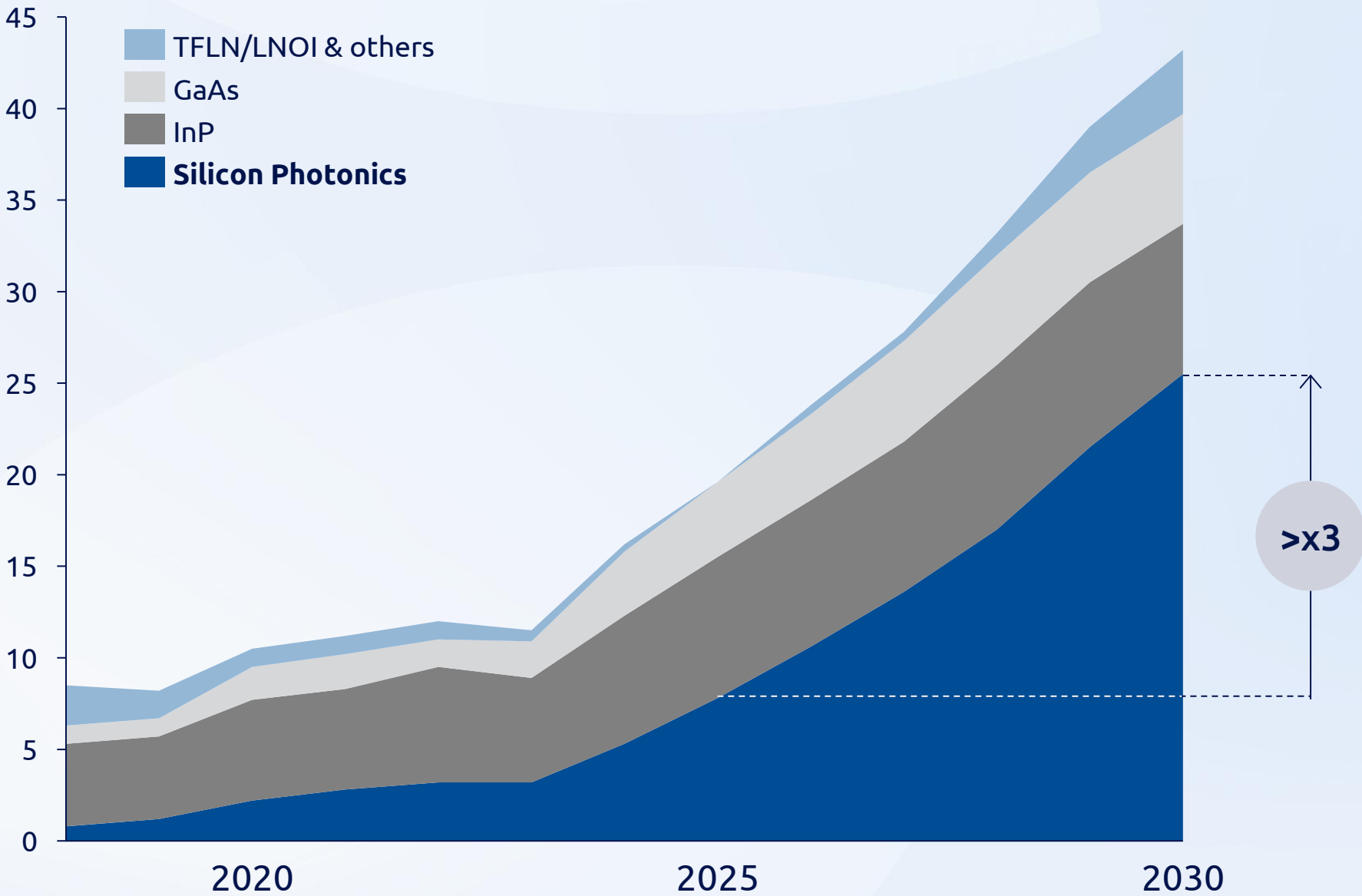
SILICON PHOTONICS IS THE PLATFORM OF CHOICE FOR OPTICAL INTERCONNECTS
SOI IS THE FOUNDATION OF SILICON PHOTONICS

CMOS

- High Density
- Low Cost
- Chip-scale Integration
- Logical functions
- Mature Ecosystem

OPTICS

- Low power dissipation
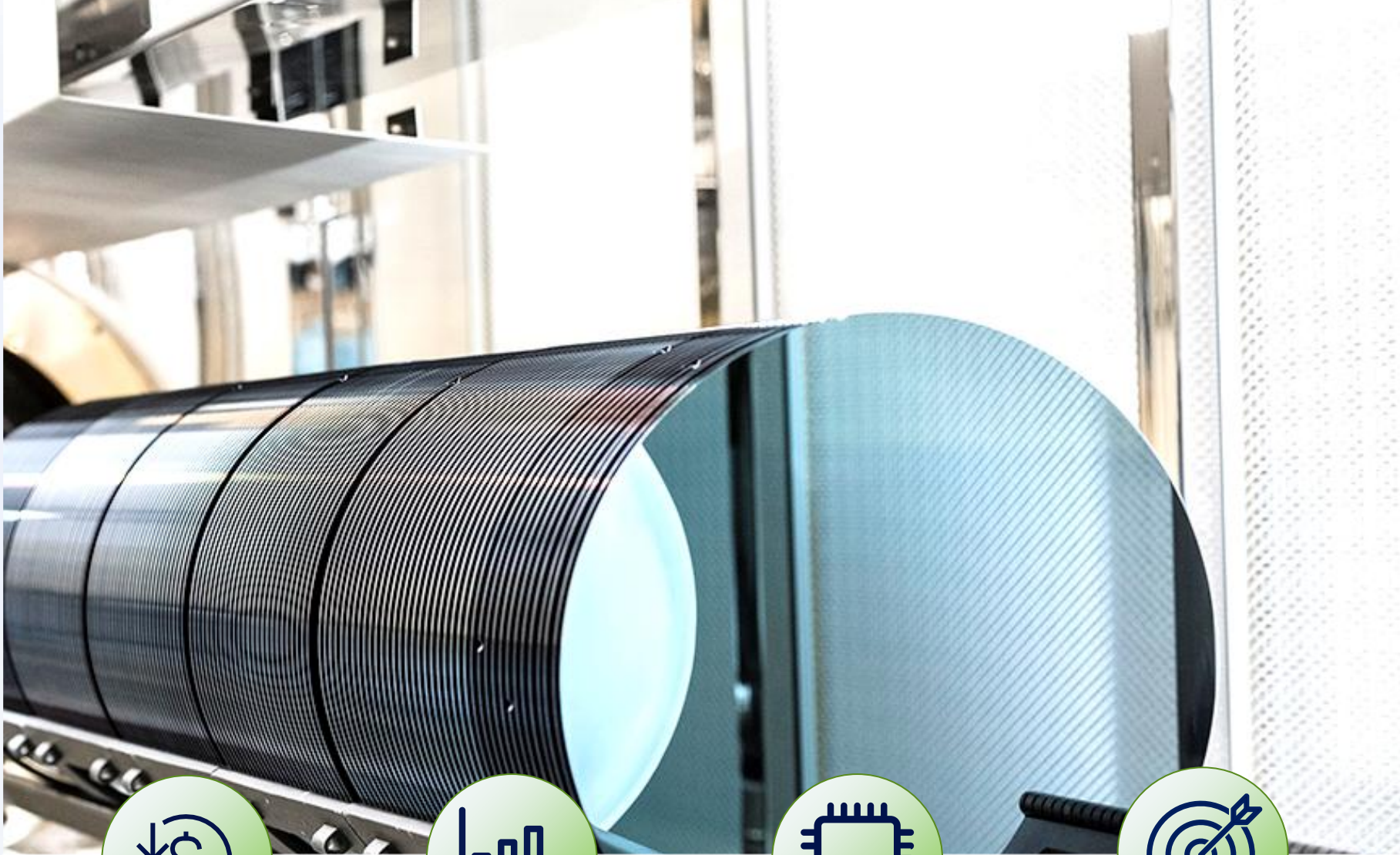- Scalable bandwidth
- Multi-wavelength
- Long reach
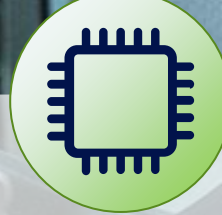- Mature infrastructure

PHOTONICS-SOI

COST — Optimized Si processes

VOLUME — Si CMOS production capabilities

PACKAGING — Si packaging compatibility

PERFORMANCE — Large bandwidth, power efficiency, high data rate, high density
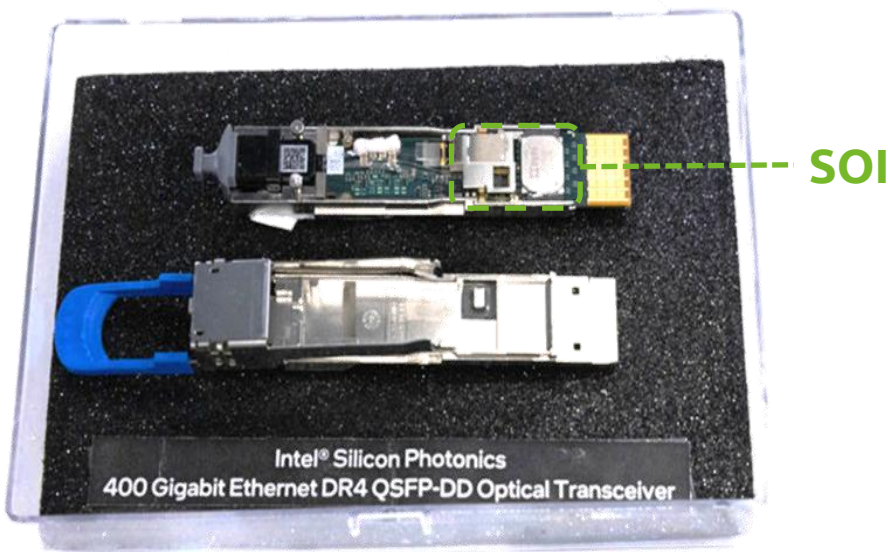
CLOUD AI PRODUCT PORTFOLIO
PHOTONICS-SOI

200mm 300mm

Mono-crystal Top Silicon
Buried Oxide
High Resistivity Silicon
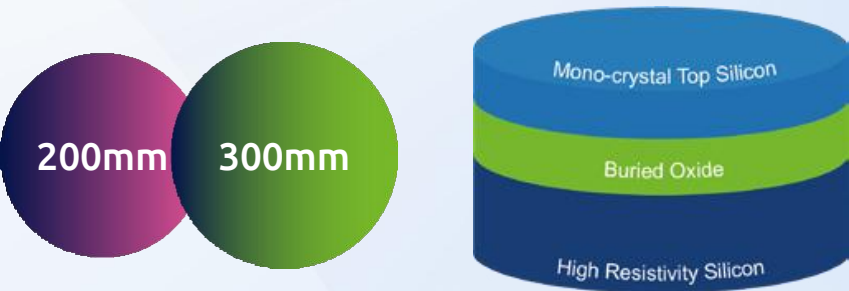
SILICON PHOTONICS INTERCONNECTS

PLUGGABLE TRANSCEIVERS

SOI

Intel® Silicon Photonics
400 Gigabit Ethernet DR4 QSFP-DD Optical Transceiver

**Silicon Photonics SOI Chipset
(400 Gb/s)**

CO-PACKAGED OPTICS (CPO)

SOI
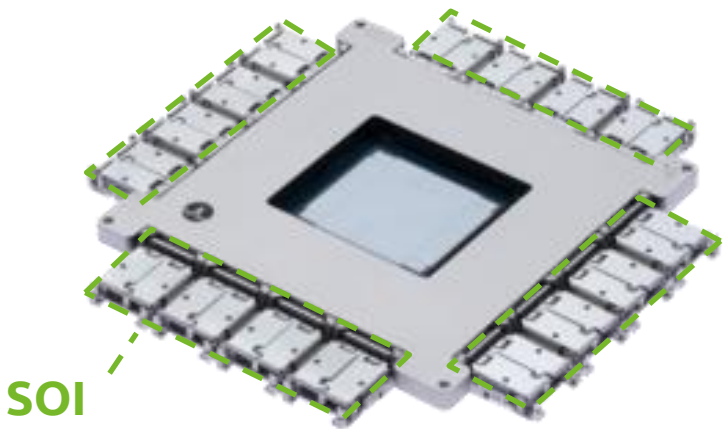
*Broadcom Multilayer CPO Switch
Tomahawk® 6 – Davisson (2025)*

**Silicon Photonics SOI Chipset
(102.4 Tb/s)**

↓

**High-density optical
interconnects**

PHOTONICS-SOI ROADMAP

PERFORMANCE SCALING →

Photon Ultra 300
**Advanced
Pluggables & CPO**

Photon Plus 300
Pluggables & CPO

Photon Ultra 200
**Advanced Pluggables
& Sensing**

Photon Plus 200
Pluggables

Photon

FUNCTIONAL & YIELD SCALING →

- PRODUCTION 200mm
- IN DEVELOPMENT 200mm
- PRODUCTION 300mm
- IN DEVELOPMENT 300mm

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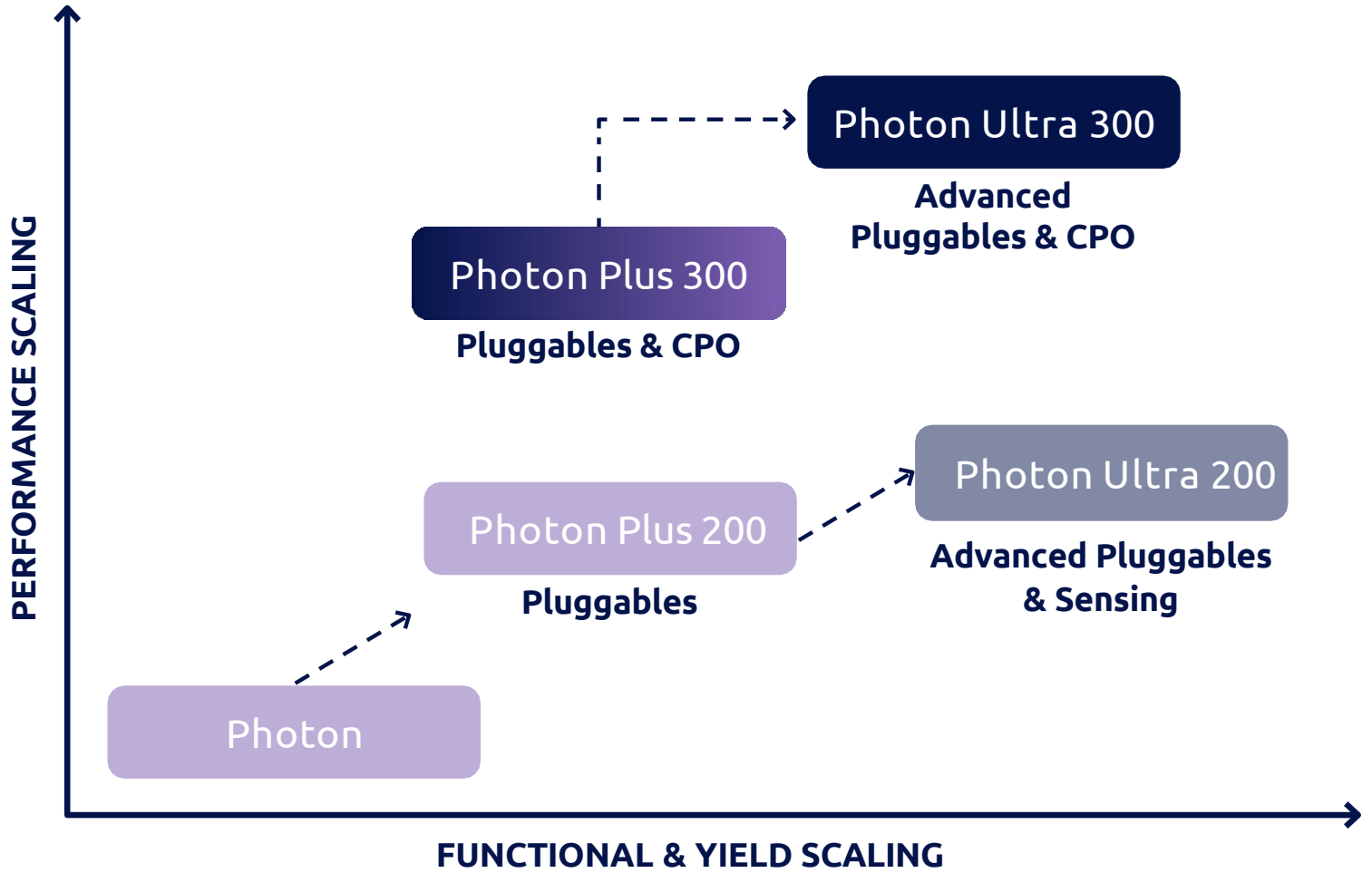
PUSHING DEVICES PERFORMANCE TO THE NEXT LEVEL

PHOTONICS-SOI MINIMIZES OPTICAL LOSSES

CONTROL OF TOP Si THICKNESS

Improved optical losses / crosstalk | High-speed optical modulators | Manufacturing Yield

OPTIMAL TOP Si ROUGHNESS

Waveguide Loss | Photodiodes Responsivity

BASE WAFER MECHANICAL STABILITY

Wafer Handling

PHOTONICS-SOI

Single-Crystal Silicon (Si)

Buried Oxide (BOX)

Handle Silicon

LOW LEVEL OF DEFECTS

TSV Driver Integration | Chip-to-Fiber Attach

HIGH PERFORMANCE OPTICAL TRANSCEIVERS ENABLED BY HIGH QUALITY ENGINEERED SUBSTRATE

Optical Amplifiers | MZI/µring modulators | Si Waveguides | GeSi, InP photodiode | Silicon Nitride devices

Surface/Edge Fiber Couplers

Light-in
Light-out

BMD: Bulk Micro Defects
TSV: Through-Silicon Vias

CLOUD AI PRODUCT PORTFOLIO
LNOI (LITHIUM NIOBATE ON INSULATOR *)

150mm 200mm

Optical LN
Buried Oxide
High Resistivity Silicon

LNOI IS TARGETING ENERGY-EFFICIENT FAST DATA TRANSFER

Cloud AI

Telecom / Space / Military

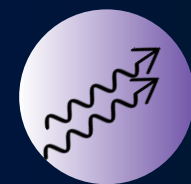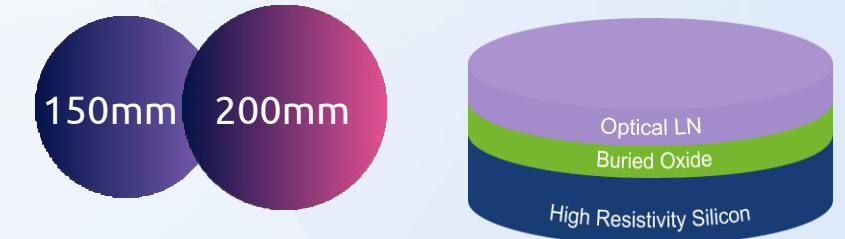Quantum

OUR LNOI SUBSTRATE ENABLES
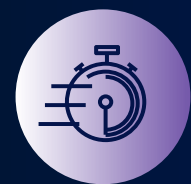
FASTER DATA TRANSFER RATE

LOWER POWER CONSUMPTION

LINEARITY (SIGNAL INTEGRITY)

PHOTONICS-Lithium rich materials ROADMAP

PERFORMANCE SCALING

LTOI 200
Datacenter & AI

LNOI 200
Datacenter & AI

LNOI 150 enhanced BOX
Datacenter & AI

LNOI 150 thick BOX
Advanced Datacenter & AI

LNOI 150 thin box
Cloud AI & Quantum

LTOI 150
Datacenter & AI

FUNCTIONAL & YIELD SCALING

IN DEVELOPMENT 150mm **PLANNED**
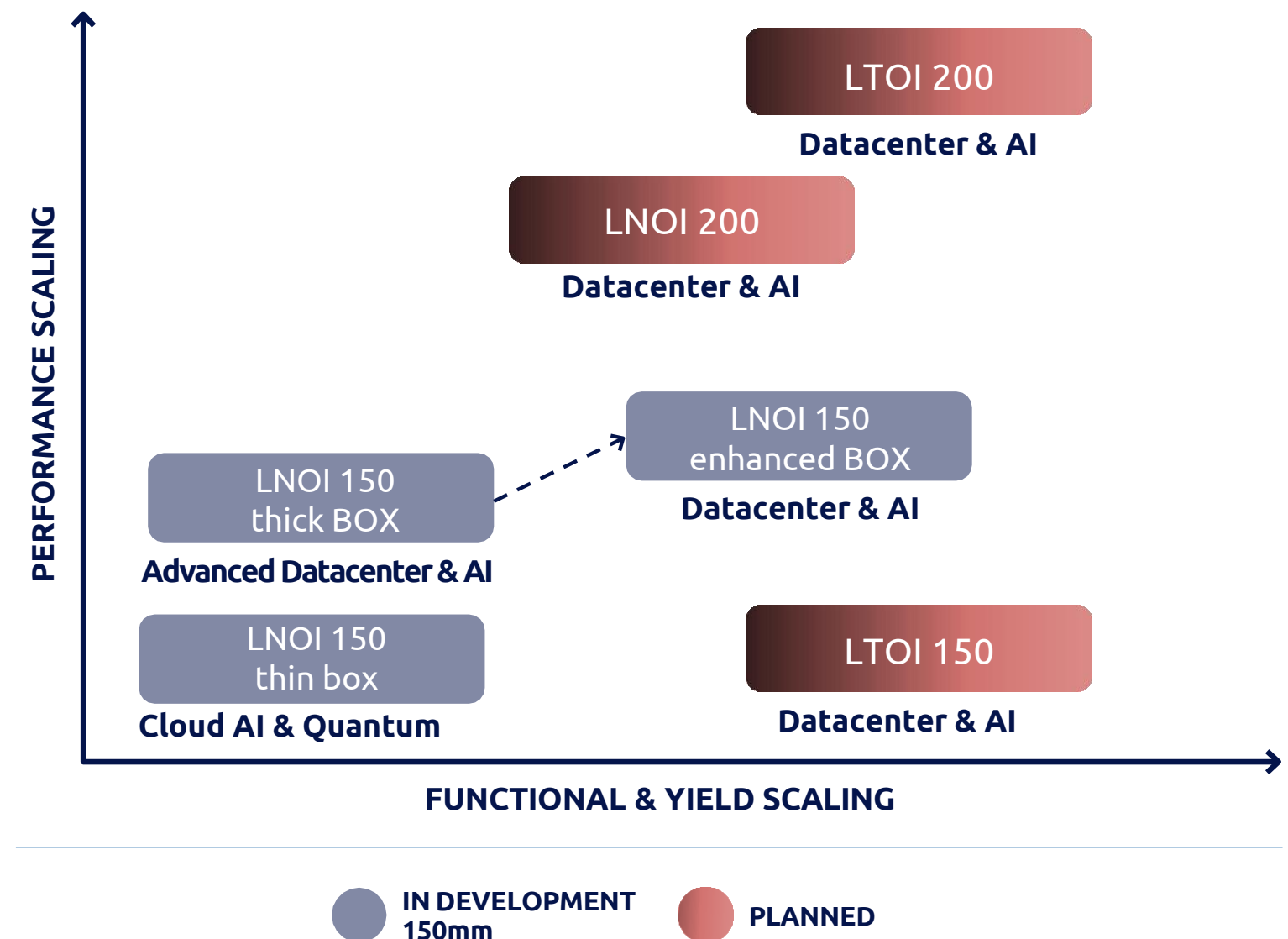
(*) LNOI is also referred to as TFLN (Thin Film Lithium Niobate)
Photo credit: © CSEM

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SOITEC ENABLES ALL OPTICAL INTERCONNECTS FROM PLUGGABLES TO CPO

Switch speed

51.2T/102.4T   115.2T

Line-speed

200G

100G   400G   800G   1.6T   3.2T

2016   2018   2020   2022   2025   2030

Transceiver Technology

Pluggables

CPO

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Photonics-SOI

LNOI
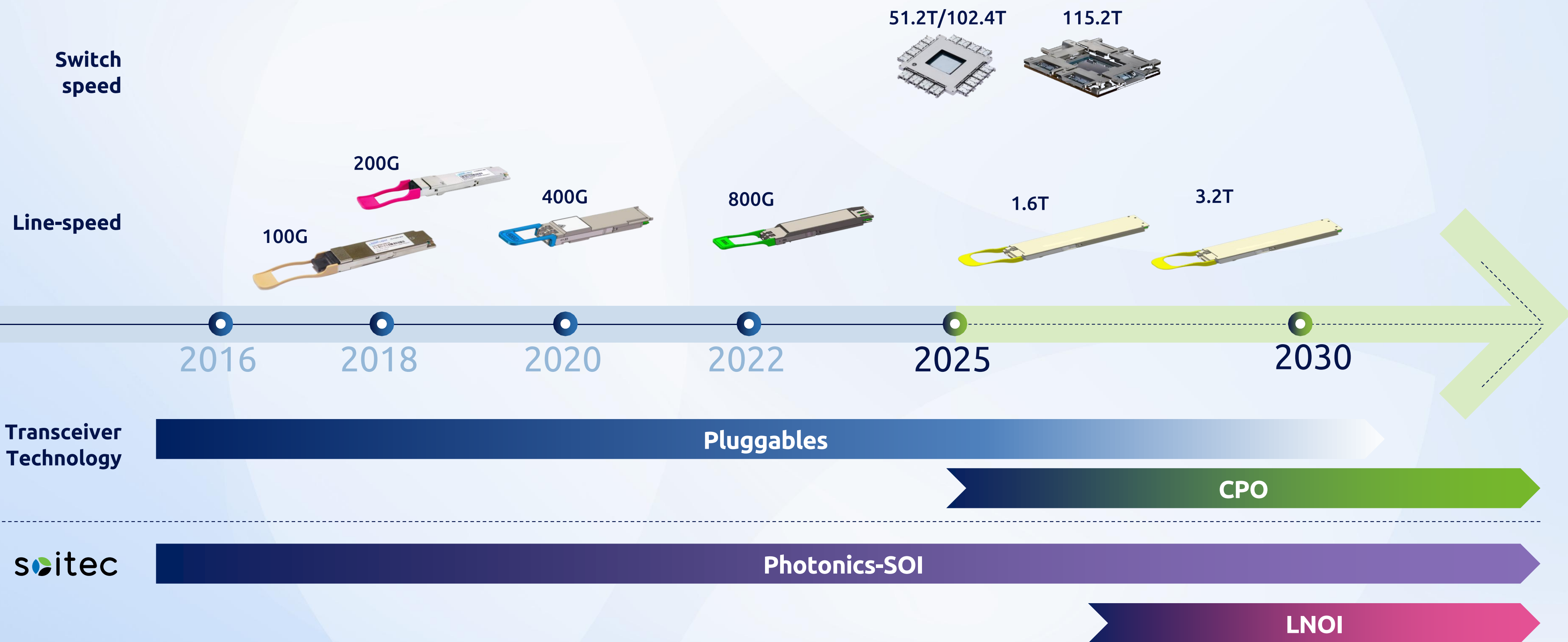
Source: Broadcom, Cisco, Nvidia

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QUANTUM DEDICATED FD-SOI

A GAME CHANGER FOR QUANTUM SPIN QUBITS

SCALABLE

Creates a scalable path toward silicon-based quantum devices

PROVEN FD-SOI PLATFORM

Integrates a proven, low-noise, and CMOS-compatible architecture

INDUSTRIAL MATURITY

Benefits from the maturity and robustness of the semi-industry

INTEGRATION of Quantum & Classical transistors
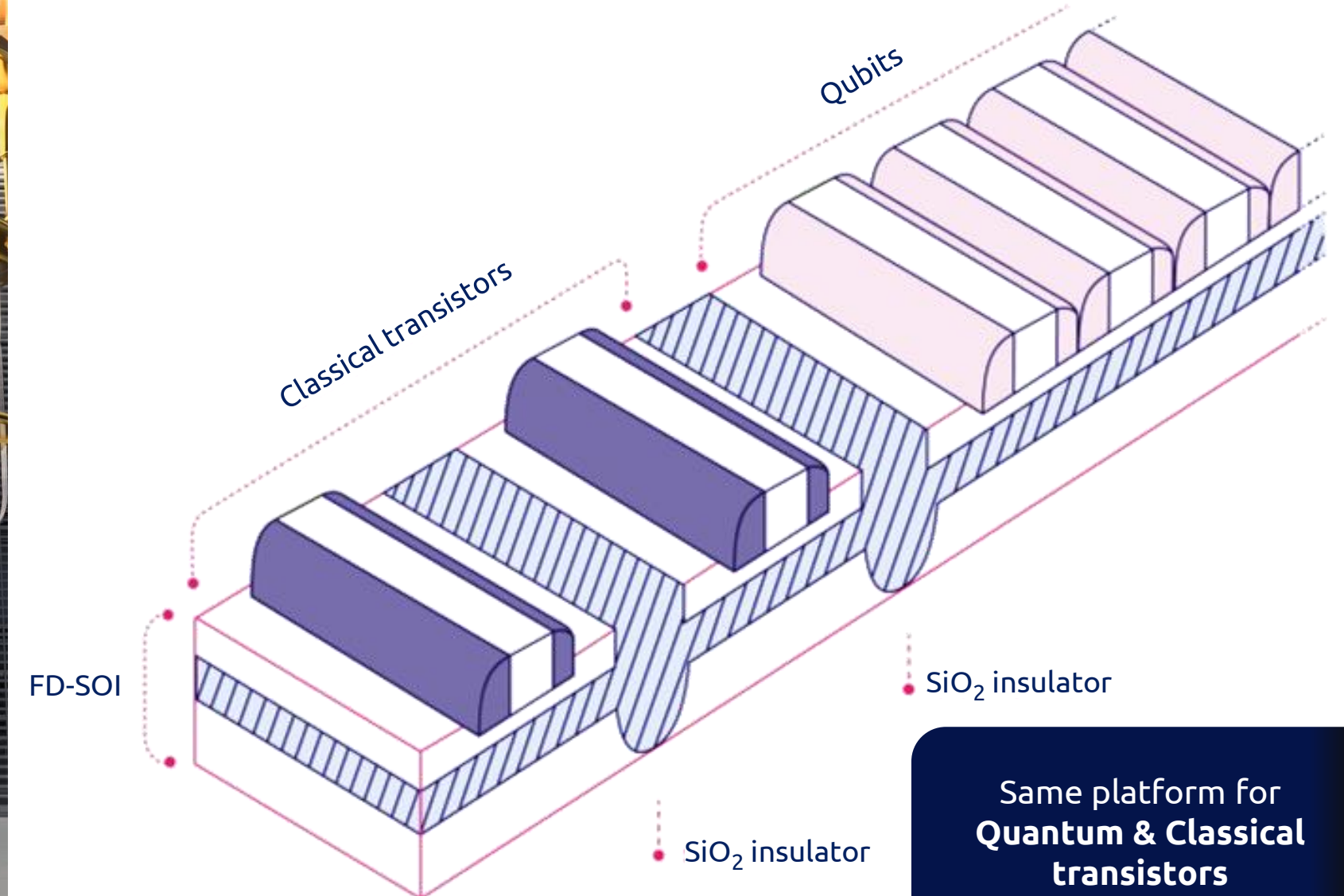
Creates a scalable path toward silicon-based quantum devices

FD-SOI – A STRONG ECOSYSTEM BUILDING UP

Source: Quobly, Soitec

quobly × **soitec** × **ST**

QUOBLY SPIN QUBITS BASED ON SOITEC FD-SOI

Qubits

Classical transistors

FD-SOI

SiO_2 insulator

SiO_2 insulator

Same platform for **Quantum & Classical transistors**

ENGINEERED SUBSTRATES FOR EDGE AI

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EDGE AI: BRINGING INTELLIGENCE CLOSER TO THE USER
CREATING NEW CHALLENGES FOR DEVICES & SUBSTRATES

NEW TECHNICAL REQUIREMENTS
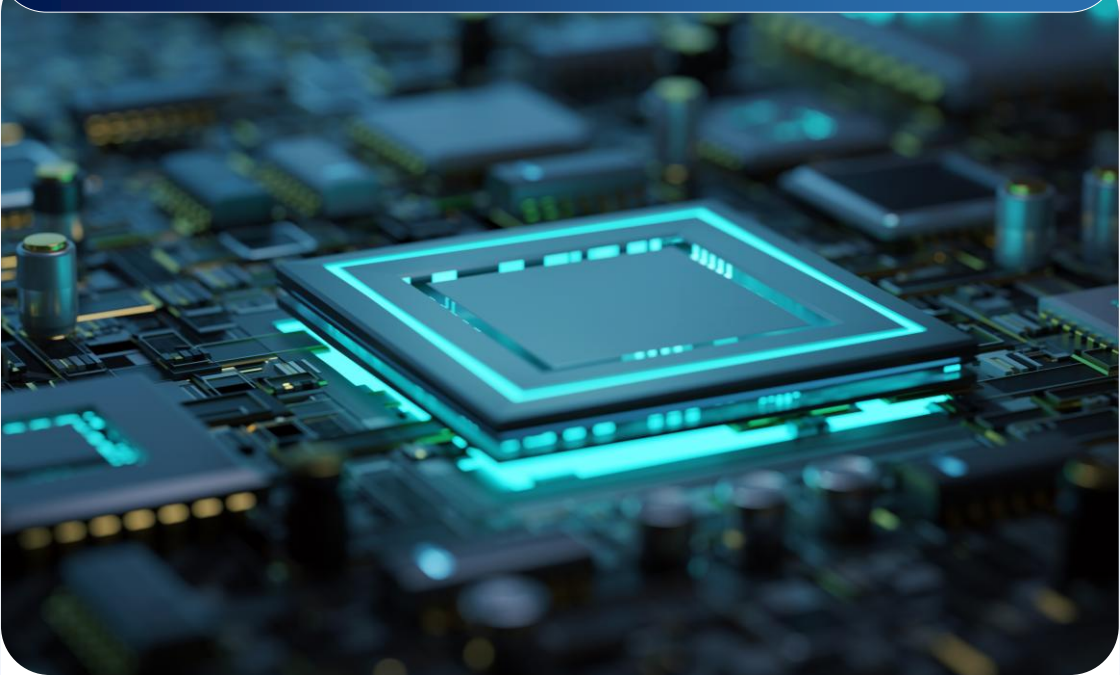
Inference at the edge

High density memory

Increased power autonomy

Reliability and robustness

MICROPROCESSOR REQUIREMENTS

High speed hardware

Optimized AI models & memory capabilities

Ultra-low standby power and Boost mode

Operation in adverse conditions

ENGINEERED SUBSTRATES: AI-NABLERS

Extended planar CMOS technology

Ultra-low leakage

Low power connectivity

Robustness against cyber attacks

AI DIGITAL LANDSCAPE FROM CLOUD TO EDGE

FD-SOI IS THE IDEAL PLATFORM FOR EMBEDDED & LOW POWER EDGE COMPUTING

Source: NICS-EFC Lab of Tsinghua University, Soitec

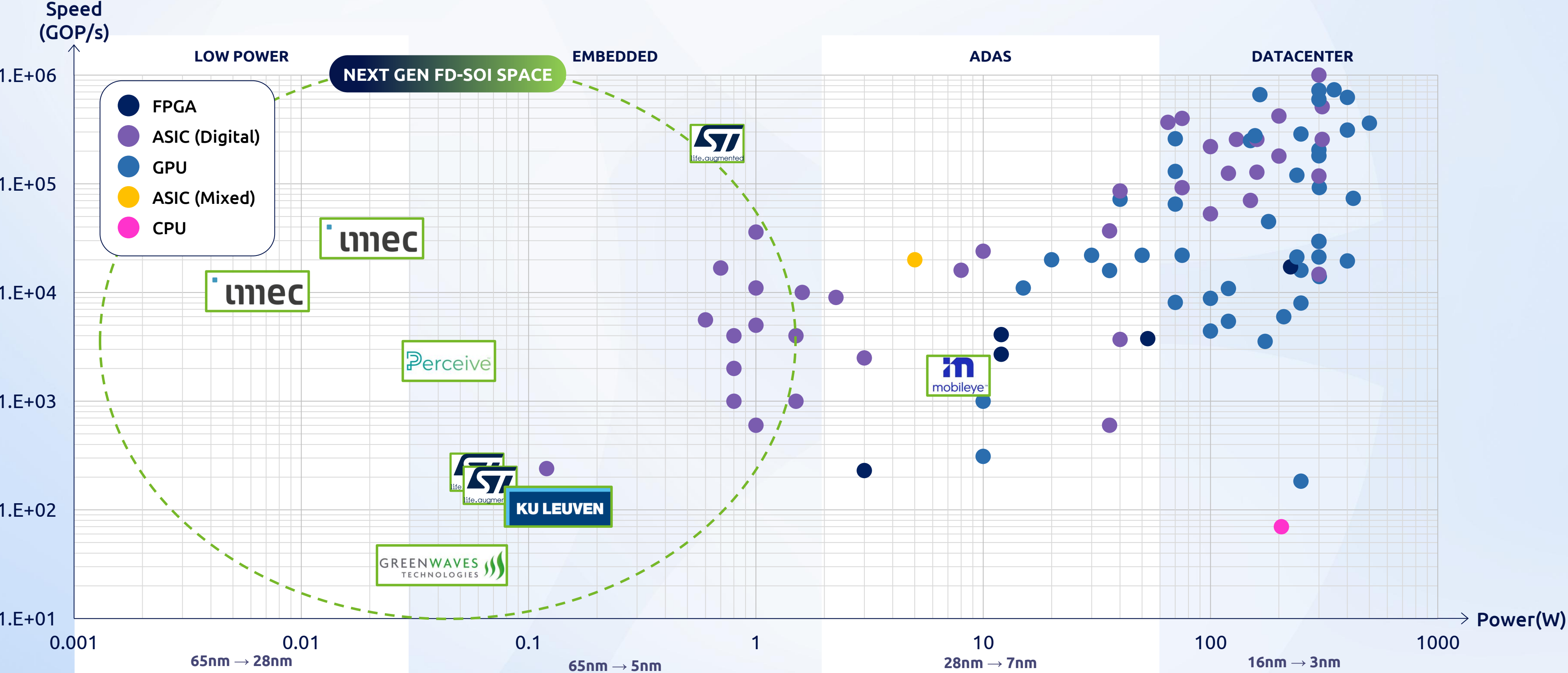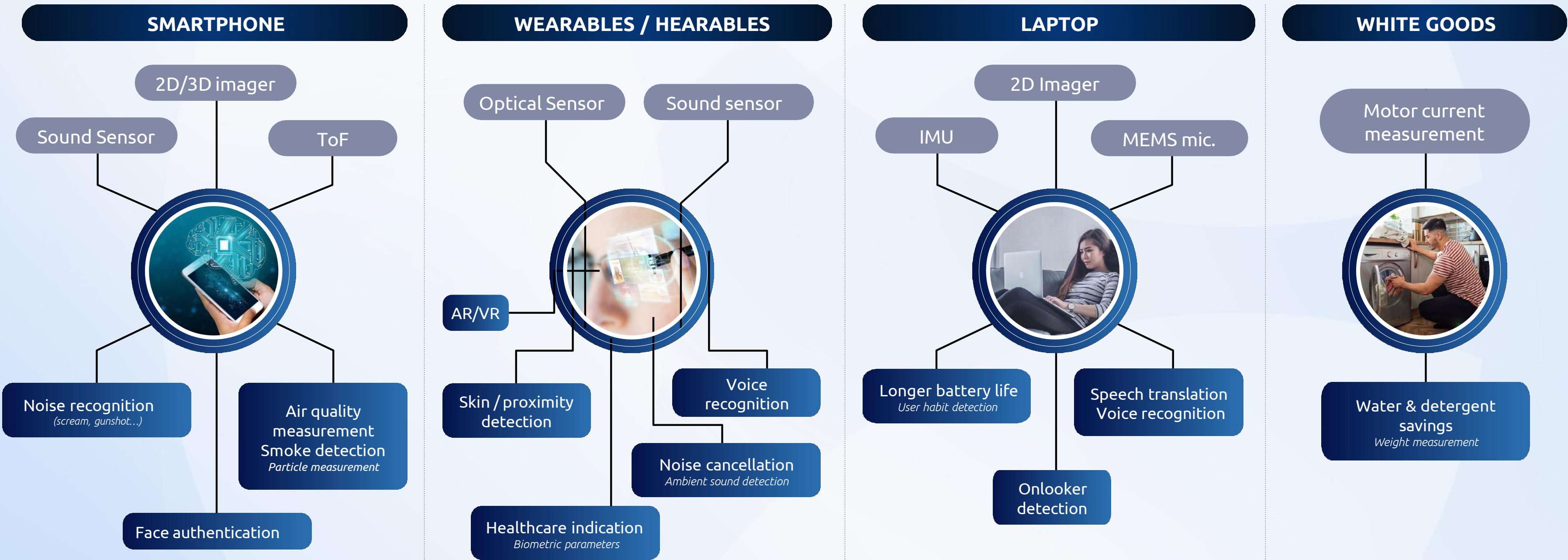# EDGE AI: OVERVIEW OF CURRENT APPLICATIONS
FROM THE EDGE TO THE ENDPOINT, AI ENHANCING MULTIPLE USE CASES

SMARTPHONE

- 2D/3D imager
- Sound Sensor
- ToF

- Noise recognition
  (scream, gunshot…)
- Air quality measurement
  Smoke detection
  Particle measurement
- Face authentication

WEARABLES / HEARABLES

- Optical Sensor
- Sound sensor
- AR/VR

- Skin / proximity detection
- Voice recognition
- Noise cancellation
  Ambient sound detection
- Healthcare indication
  Biometric parameters

LAPTOP

- 2D Imager
- IMU
- MEMS mic.

- Longer battery life
  User habit detection
- Speech translation
  Voice recognition
- Onlooker detection

WHITE GOODS

- Motor current measurement

- Water & detergent savings
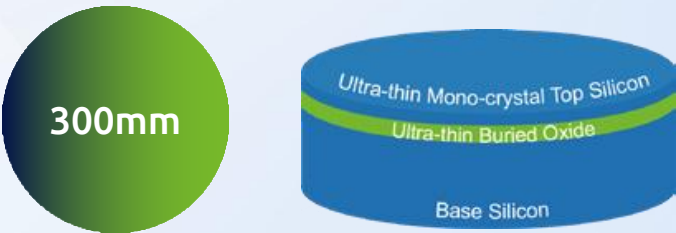 *Weight measurement*

AI AT THE EDGE ENABLES

- Lower latency
- Power saving
- Enhanced user experience
- Cybersecurity
- Greater privacy

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EDGE AI: FOCUS ON WEARABLES
MCU FOR SMARTWATCH TO MAXIMIZE BATTERY LIFE

300mm

Ultra-thin Mono-crystal Top Silicon
Ultra-thin Buried Oxide
Base Silicon

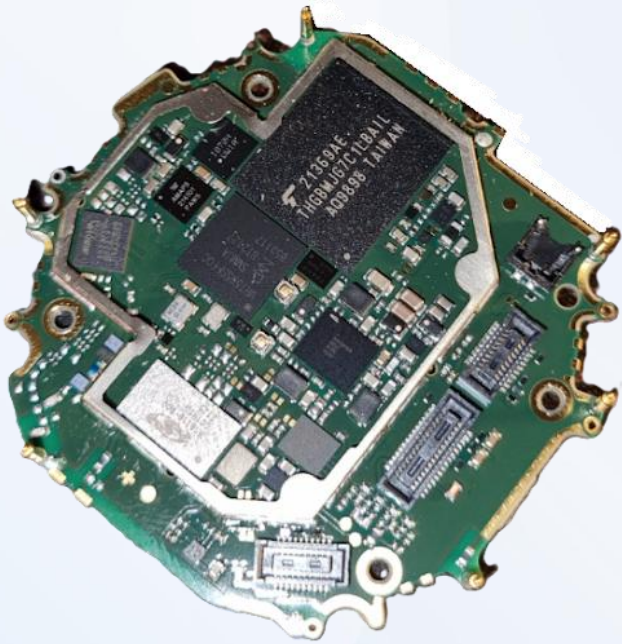**EDGE AI PRODUCT** → **PCB BOARD** → **MICROCONTROLLER** → **ENGINEERED SUBSTRATE**
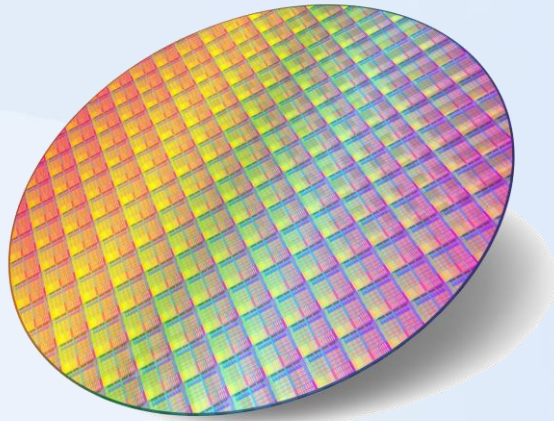
i.MX RT500

Garmin fēnix® 8 smartwatch

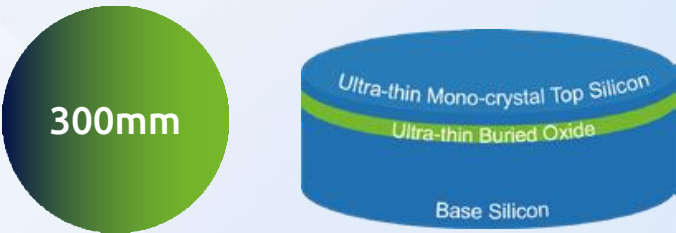Edge board

Packaged MCU ~50mm²

FD-SOI Die size >20mm²

Source: Garmin, NXP, Soitec estimate

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EDGE AI: FOCUS ON ADVANCED WEARABLES
MCU COPROCESSOR IN AI SMART GLASSES TO MAXIMIZE BATTERY LIFE

300mm

Ultra-thin Mono-crystal Top Silicon
Ultra-thin Buried Oxide
Base Silicon

AI SMART GLASSES

Meta Ray-Ban Display

AI SMART GLASSES REQUIREMENTS

Compact form factor / Light
Processing capability
Long battery life

HETEROGENEOUS COMPUTE ARCHITECTURE

HIGH-PERFORMANCE AR PROCESSOR

Snapdragon AR2 Gen 1

Qualcomm Snapdragon AR2 Gen 1

High-performance application processor supporting high-resolution video, neural network processing, and wireless connectivity

➕

ULTRA-LOW POWER CROSSOVER MCU

NXP i.MX RT700 MCU
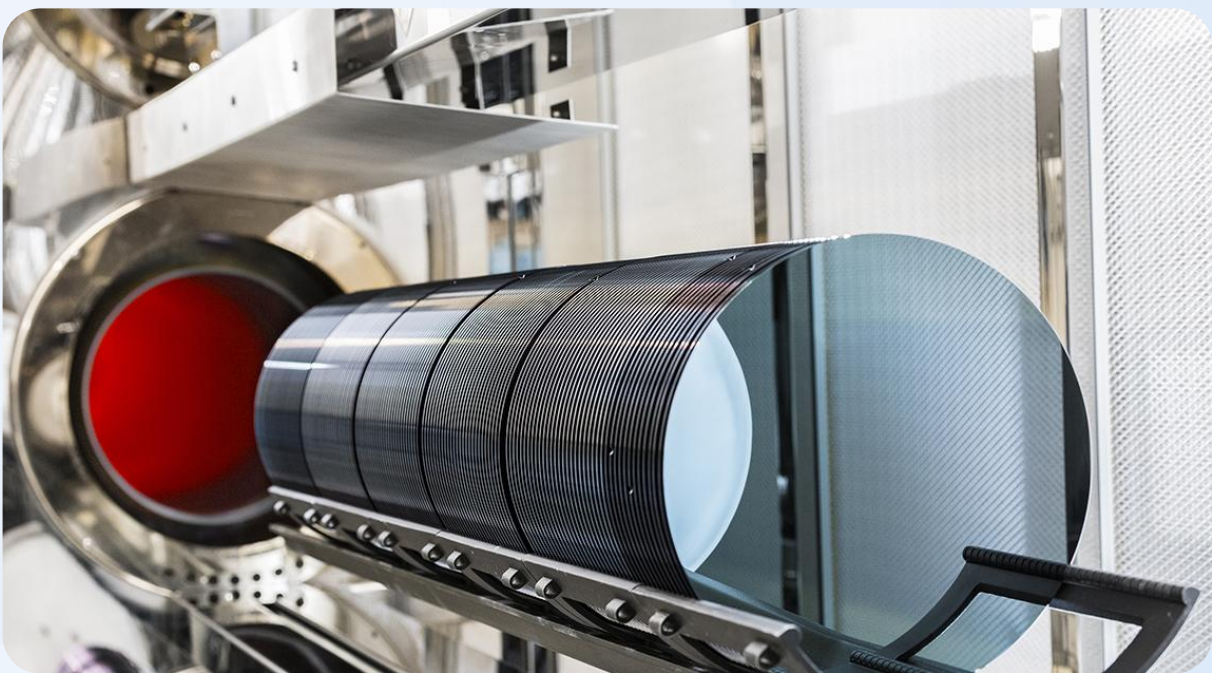
Lower active and standby power coprocessor to enable always-on features such as voice wake-up, music playback, and calls

built on 28nm FD-SOI

ENGINEERED SUBSTRATE

FD-SOI BENEFITS FOR AI SMART GLASSES

Energy efficiency / low-leakage

Always-on / on-demand performance

Low power consumption

Greater integration / compacity

Source: Meta, NXP, Qualcomm

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FD-SOI FOR EDGE COMPUTING
INDUSTRY WIDE ADOPTION DOWN TO 18nm

300mm

Ultra-thin Mono-crystal Top Silicon
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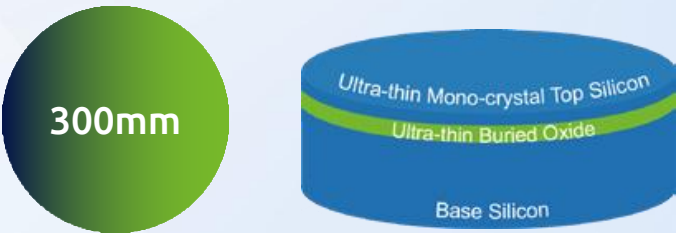
FD-SOI BENEFITS ALL WEARABLE APPLICATIONS WITH BETTER PERFORMANCES

Smart Home Devices

Wearables

Environmental Smart Sensors

Medical IoT
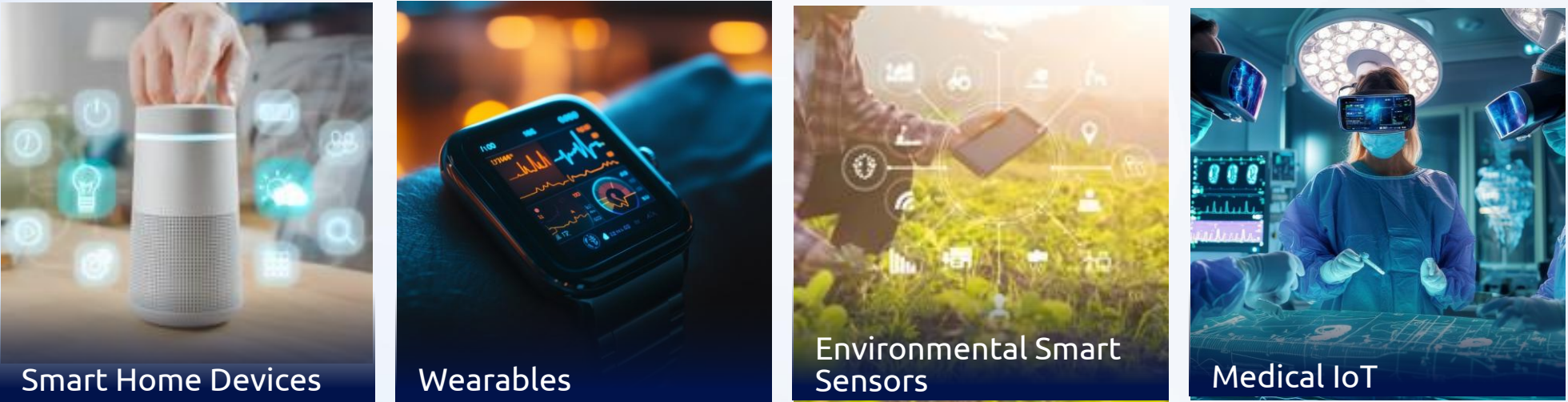
OUR FD-SOI SUBSTRATE ENABLES

LOWER ACTIVE POWER CONSUMPTION - ALWAYS ON

PERFORMANCE ON DEMAND

ROBUST ENERGY HARVESTING 'ZERO POWER' CAPABILITIES

LOWEST-COST PROCESSING (INFERENCES-PER-WATT-PER-$)

ROBUSTNESS TO CYBER ATTACKS

FD-SOI ROADMAP

POWER EFFICIENCY, PERFORMANCE AND CONNECTIVITY

eSoC.3
12nm & below

eSoC.2
28nm → 18nm

Gen1.1
65nm → 22nm

TECHNOLOGY SCALING

● PRODUCTION   ● IN DEVELOPMENT

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AI-NABLERS
EXPANDING PRODUCT PORTFOLIO TO ENABLE FUTURE AI DEVELOPMENTS

SUBSTRATE	AI-NABLER	ACTIVE LAYER							
		Silicon	Piezo	SiC	InP	GaN	GaAs	Ge	Others
Silicon or SOI		●	●	●	●	●	●	●	Diamond GaOx / 2D materials
Sapphire		●			●	●	●	●	
SiC or polySiC				●		●			
GaAs					●		●		
Device wafer		●	●						
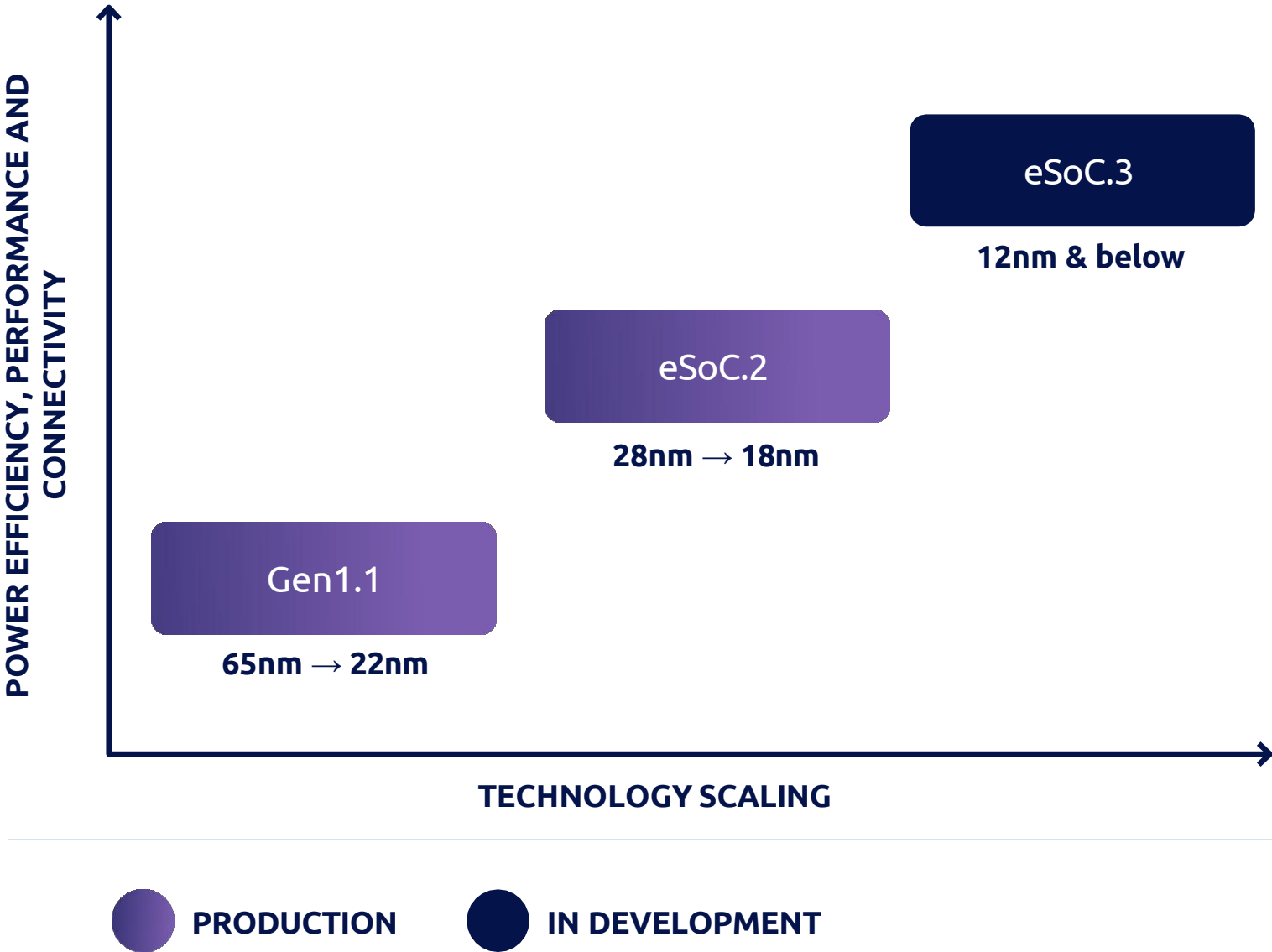
AI-NABLERS
EXPANDING PRODUCT PORTFOLIO TO ENABLE FUTURE AI DEVELOPMENTS

ACTIVE LAYER

SUBSTRATE / AI-NABLER	Silicon	Piezo	SiC	InP	GaN	GaAs	Ge	Others
Silicon or SOI	Low power Transistor isolation Radiation hardness — Edge AI, 4G/5G, Datacenter, Imager	High performance RF filters — 4G/5G	Co-integration — Quantum	Co-integration Scalable to 300mm High performance — 6G, Photonics, Imager	PA performance Co-integration — 5G/6G, smartphones	Co-integration Scalable to 300mm — Optoelectronics	Co-integration Scalable to 300mm High mobility — Optoelectronics	Better performance — Power electronics; Better performance — HPC, IoT
Sapphire	Transistor isolation Radiation hardness — 3G/4G			Co-integration High performance — Optoelectronics	High performance — microLEDs	Co-integration High performance — Optoelectronics	Co-integration High performance — Optoelectronics	
SiC or polySiC			Better performance Higher yield Greener technologies — Power electronics		PA performance Co-integration — 5G/6G, baseband			
GaAs				Optical performance — Optoelectronics		Optical performance — Optoelectronics		
Device wafer	Uniformity Crystal quality SoC integration — 3D Sequential integration; Uniformity Crystal quality Yield — Sensors, Actuators							

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THANK YOU

GLOSSARY

ASIC (Application-Specific Integrated Circuit): A custom-designed chip optimized for a specific function or application.

ADAS (Advanced Driver Assistance System): A suite of technologies that enhance vehicle safety and driving through automation and alerts.

AR/VR (Augmented Reality / Virtual Reality): Technologies that overlay digital content on the real world (AR) or immerse users in a virtual environment (VR).

CPO (Co-Packaged Optics): Integration of optical components and silicon in the same package to reduce power and increase bandwidth.

CPU (Central Processing Unit): The primary processor that executes instructions and manages tasks in a computing system.

DRAM (Dynamic Random Access Memory): A type of volatile memory used for high-speed data access in computing systems.

GPU (Graphics Processing Unit): A processor optimized for parallel data tasks, widely used in graphics rendering and AI.

IoT (Internet of Things): A network of connected devices that collect, exchange, and act on data via the internet.

MCU (Microcontroller): A compact integrated circuit used to control specific functions in embedded systems.

ML (Machine Learning): A subset of AI that enables systems to learn and improve from data without explicit programming.

xPU: A general term for processing units, covering a range of specialized and general-purpose chips.