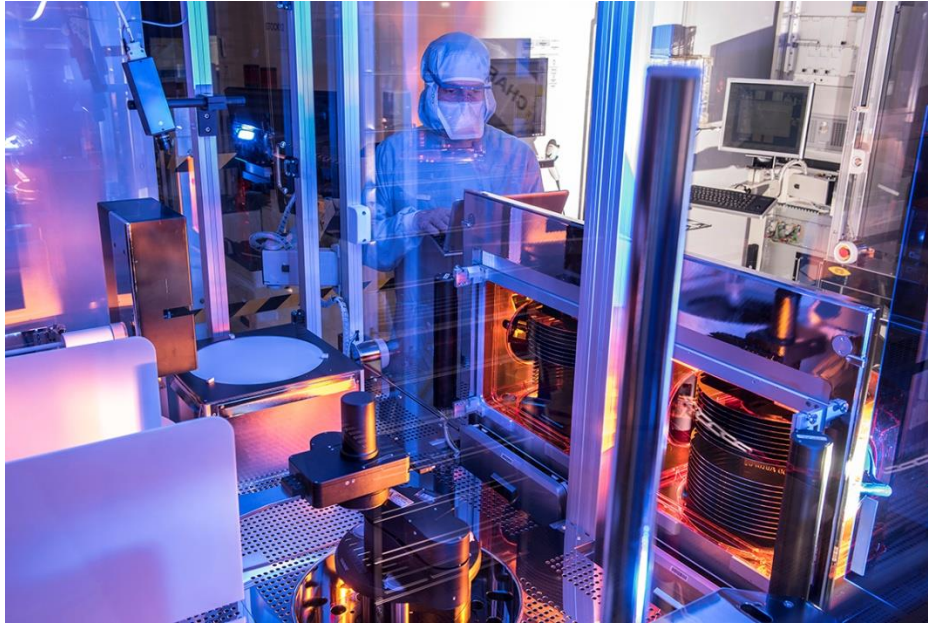


White Paper

RF-SOI Wafer Characterization



Abstract

While new network standards such as LTE Advanced require RF devices in the front-end module to perform with higher linearity, they increase the burden at all levels of the value chain to provide better RF products: from system design and RF integrated circuits down to engineered substrate design.

This paper describes how Soitec's innovative metrology on its wafers is able to predict the RF performance of final devices manufactured on Soitec RFeSI™ substrates.

Abbreviations

CPW	Coplanar Waveguide
RFeSI	Radio-Frequency enhanced Signal Integrity
HD2	2nd Harmonic Distortion
HQF	Harmonic Quality Factor
LTE	Long-Term Evolution
RF-SOI	Radio-Frequency Silicon-on-Insulator
SOI	Silicon-on-Insulator
SRP	Spreading Resistance Profiling



Introduction

The demand for more bandwidth to transfer ever-increasing amounts of data (video, photos and data files) between a network and mobile phones pushes network operators to strive for better performance. The first milestone was 3G, 4G is now being adopted and the next step will be LTE Advanced, then 5G.

These network standards require mobile phones to support more bands, higher frequency bands, emission and reception on adjacent bands with downlink and uplink carrier aggregation.

To support a whole range of network configurations, the front-end module is becoming more and more complex. The integrated devices for front-end modules require advanced RF design techniques associated with carefully tuned manufacturing processes as well as specific substrates compatible with RF performance requirements.

Today the vast majority of RF switches is built on RF-SOI, which has replaced GaAs substrates for those applications. RF-SOI also is used in power amplifiers and antenna tuners.

To address the different communication standards and functions used in front-end modules, Soitec, the leader in SOI technology, has developed two flavors of RF-SOI products – Soitec HR-SOI and Soitec RF Enhanced Signal Integrity™ (RFeSI) SOI – both of which are compatible with standard CMOS processes. While standard HR-SOI is capable of meeting 2G or 3G requirements, Soitec RFeSI SOI can achieve much higher linearity and isolation specifications, allowing designers to address some of the most stringent LTE requirements. This paves the way for integrating more functions on a device with better RF performance at competitive cost.

To quantify the performance one can expect from a Soitec RFeSI SOI substrate, Soitec developed a characterization method based on spreading resistance profiling (SRP), which can predict the 2nd harmonic distortion (HD2) performance of a coplanar waveguide. This metrology is used today throughout the Soitec RFeSI product line to ensure the substrates will enable the expected RF performance in the finished devices.

Bandwidth's impact on RF front-end module complexity

Because high-end mobile devices offer users more content and applications than lower end devices, the traffic usage in smart phones is 49 times higher than in basic-feature phones (Figure 1) [Ref 1].



Figure 1: High-End Devices Significantly Multiply Traffic

With the wide adoption of smart phones, we should expect the average traffic per smart phone to increase by 10X between 2013 and 2018 with mobile video generating more than 69 percent of the traffic (Figure 2). By 2018, the average traffic in a 4G smart phone will reach 5,371 MB per month compared to 529 MB per month in 2013 on a standard smart phone.

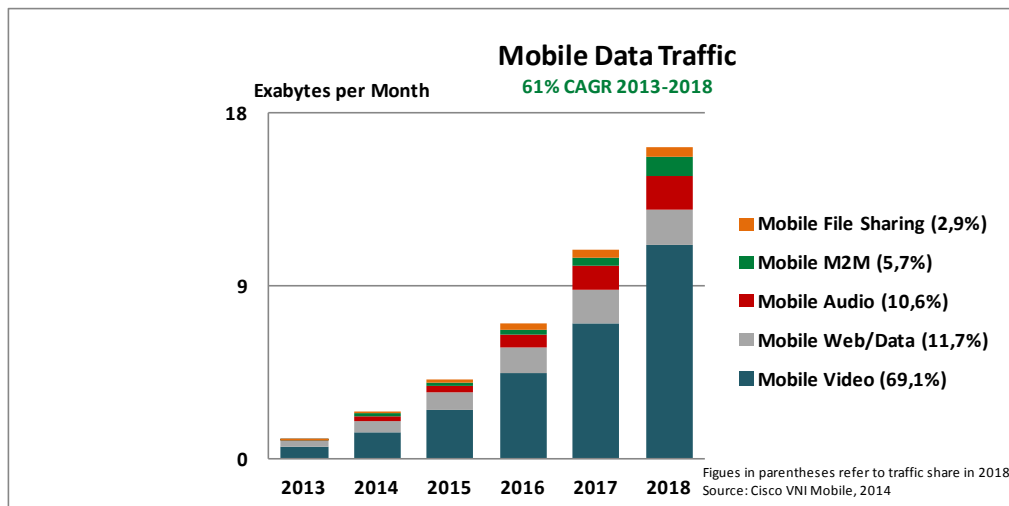


Figure 2: Mobile Video Will Generate Over 69 Percent of Mobile Data Traffic by 2018

In the same period, the average smart phone connection speed will almost double from 4 Mbps to more than 7 Mbps (Figure 3).

	2013	2013	2014	2015	2016	2018	CAGR 2013–2018
Global							
Global speed: All handsets	1,387	1,676	1,908	2,147	2,396	2,509	13%
Global speed: Smartphones	3,983	4,864	5,504	6,132	6,756	7,044	12%
Global speed: Tablets	4,591	5,584	6,298	6,483	8,018	8,998	14%

Source CISCO VNI Mobile, 2014

Figure 3: Projected Average Mobile Network Connection Speeds (in Kbps) by Region

With data consumption increasing along with higher bandwidth requirements, more advanced technologies – such as LTE, LTE Advanced, Wi-Fi 802.11.ac and beyond – are needed to offer higher data rates of 1 Gbps and greater on wireless networks. These new standards are emerging already (Figure 4).

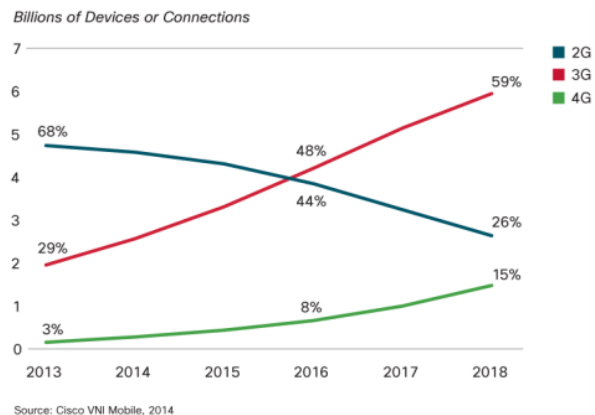


Figure 4: Global Mobile Devices and Connections by 2G, 3G and 4G

The advent of more advanced standards requires more frequency bands to achieve the needed throughput associated with tougher linearity requirements (Figure 5).

Network	Linearity (IIP3 in dBm)
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

Source: Intel Mobile Corporation, "Challenges for Radios Due to Carrier Aggregation Requirements," by Larry Schumacher, Nov. 6, 2012).

Figure 5: Linearity Requirements by Network Standard

At the front-end module level, this will translate into increased complexity in the front-end module and multiple changes for each main function (Figure 6 and 7).

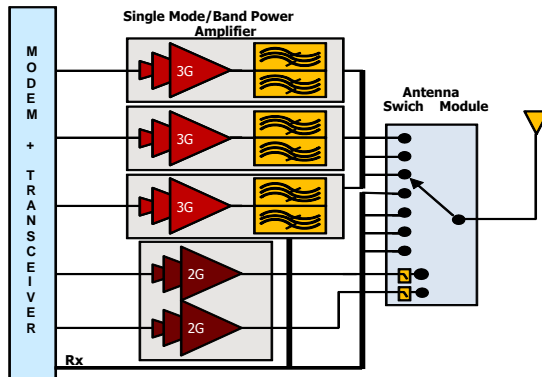


Figure 6: Example of Front-End Module Block Diagram for 3G

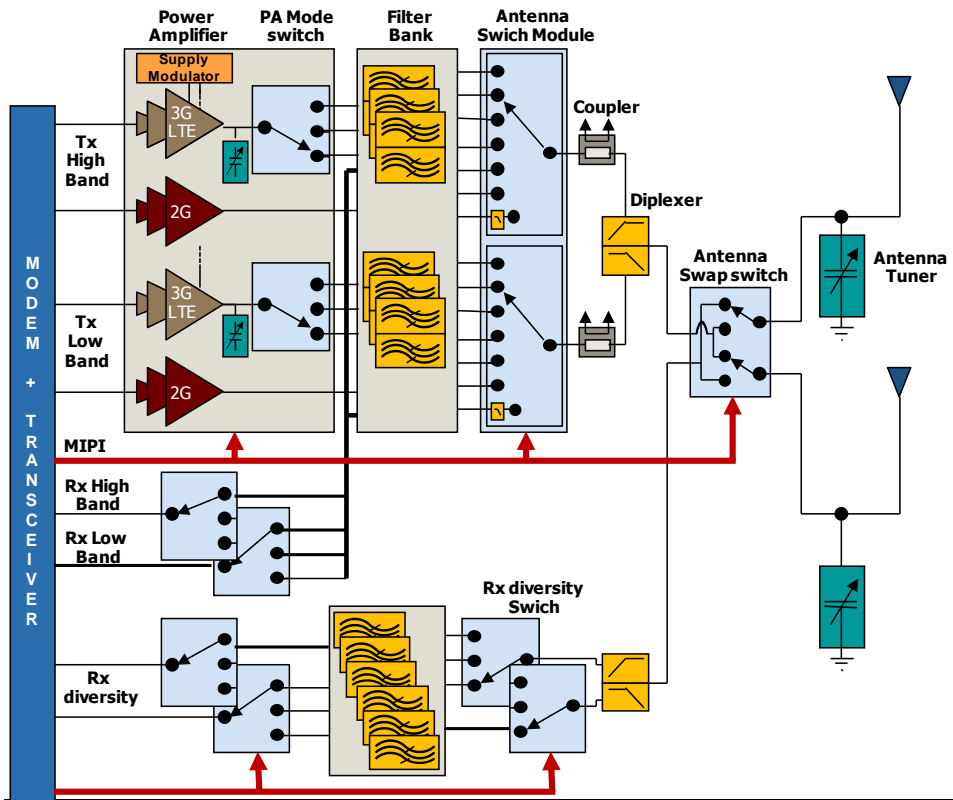


Figure 7: Example of Front-End Module Block Diagram for LTE

This will mean:

- A proliferation of switches on top of the antenna switch including diversity, power-mode and antenna-swapping switches
- Advanced, tunable power-amplifier architectures to achieve compact and cost-effective multi-mode, multi-band transmission in a single broadband power amplifier

- Advanced power management: with an envelope-tracking system approach, the efficiency of broadband power amplifiers will be close to or as good as that of single-band power amplifiers
- Advanced wide-band antenna: with an antenna-tuner system performing either impedance matching and/or aperture tuning, an antenna can efficiently cover bands with frequencies from 700 MHz to 3.5 GHz with optimum efficiency and a smaller footprint

Those front-end modules need to support more bands, higher frequency bands from 700 MHz to 3.5 GHz, larger bands from 20 MHz to 100 MHz and carrier aggregation downlink and uplink, sometimes on adjacent bands.

To meet the required performance, many changes are happening at all levels including systems, architectures, design, manufacturing processes and devices down to the substrates. The substrates on which devices are manufactured have a significant impact on the level of performance that the final devices will be capable of achieving [Ref 6]. RF-SOI has emerged as today’s substrate of choice. These wafers produced with Soitec’s Smart Cut™ technology on a high-resistivity base are used in the majority of smart phones manufactured today, making them the mainstream engineering substrates for switches. In addition, RF-SOI is emerging as the preferred solution for on-chip integration of advanced multi-mode, multi-band power amplifiers with switches.

Addressing the next RF standards with RF-SOI

Soitec’s HR-SOI product line employs a standard high-resistivity base. Compared to standard SOI, HR-SOI dramatically reduces both resistivity losses and crosstalk and has been adopted to integrate switches for 2G and 3G applications. While HR-SOI substrates are well suited for these applications, the need for higher linearity and increased integration requires a step-up in substrate capabilities.

To reach the next step in performance and to address 4G requirements, Soitec and Université Catholique de Louvain (UCL) developed a technique to add a trap-rich layer underneath the buried oxide (Figure 8) [Ref 3– 8].



Figure 8: Soitec RFeSI Wafer

Using a set of very specific patents, Soitec applies its proprietary technology and accumulated knowledge to build its RFeSI SOI product line.

Another major innovation with Soitec RFeSI SOI products comes from the ability to predict the RF harmonic distortion performance of the substrate immediately after the RFeSI SOI substrates are

fabricated and before any devices are manufactured on them. This prediction is provided through the harmonic quality factor (HQF) parameter.

RF metrology: Harmonic quality factor parameter

Soitec has developed this unique and proprietary metrology to characterize its RFeSI SOI wafers. It predicts the expected RF linearity of finished ICs. As we will see, HQF correlates with the second harmonic distortion generated from a 900-MHz signal applied to a coplanar waveguide (CPW) deposited on the substrate.

Methodology

First, CPWs are implemented by depositing aluminum metal lines on the buried oxide of Soitec RFeSI SOI wafers (Figure 9).

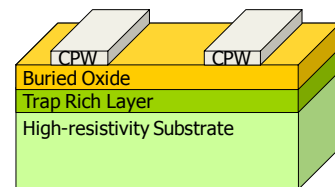


Figure 9: Metal Lines Deposited on the Buried Oxide of eSI Wafers

Then a 900-MHz fundamental tone is applied on one end of the CPW line and the HD2 signal is measured at the other end (Figure 10), providing a value of the HD2 generated by the substrate.

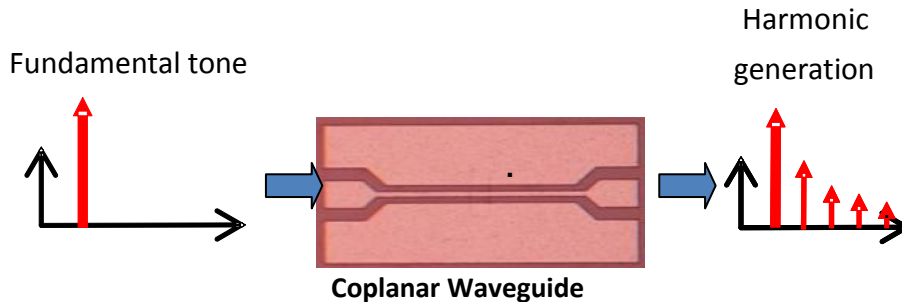


Figure 10: Harmonic Generation through Coplanar Waveguide

Figure 11 represents different HD2 measurements across different input powers and different types of substrates. At 15-dBm input power, Soitec RFeSI SOI wafers exhibit an HD2 attenuation measurement that is 25 dB better than with HR-SOI wafers.

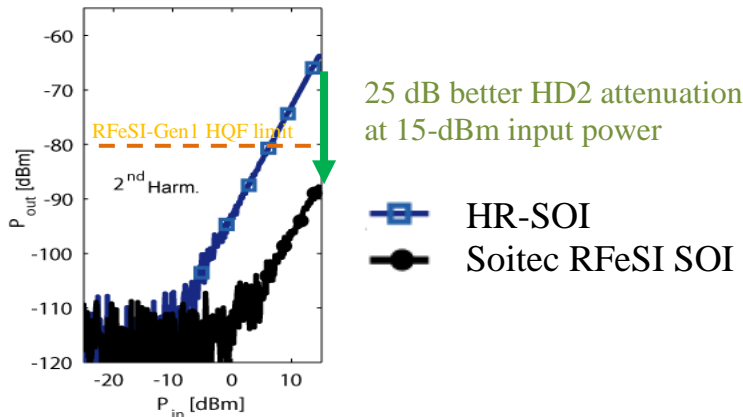


Figure 11: 2nd Harmonic Distortion at Different Input Powers on HR-SOI and Soitec RFeSI Substrates

Using the same wafers, a SRP technique [Ref 2] was used to measure the resistivity of the material at different depths under the buried oxide (Figure 12).

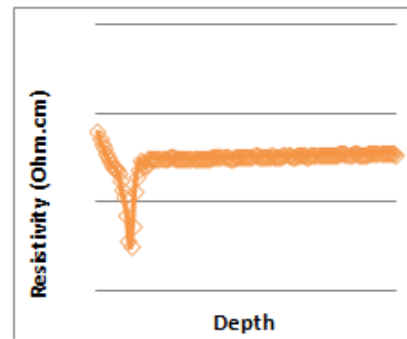
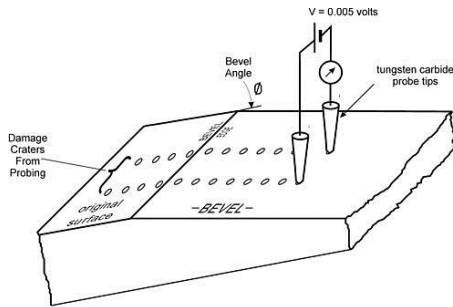


Figure 12: Spreading Resistance Profiling and Example of Results – SRP Plot

The series of measures was then computed using a proprietary algorithm tuned to match the HD2 values from those wafers at 15dBm input power. The algorithm takes into account the resistivity of the substrates weighted by the depth of the measure; the deeper in the substrate, the less weight the measure will carry in the algorithm. The result of this computation is called HQF.

Results

Several wafers with different HD2 at 15dBm input power and HQF characteristics were measured and we were able to correlate those two parameters (Figure 13).

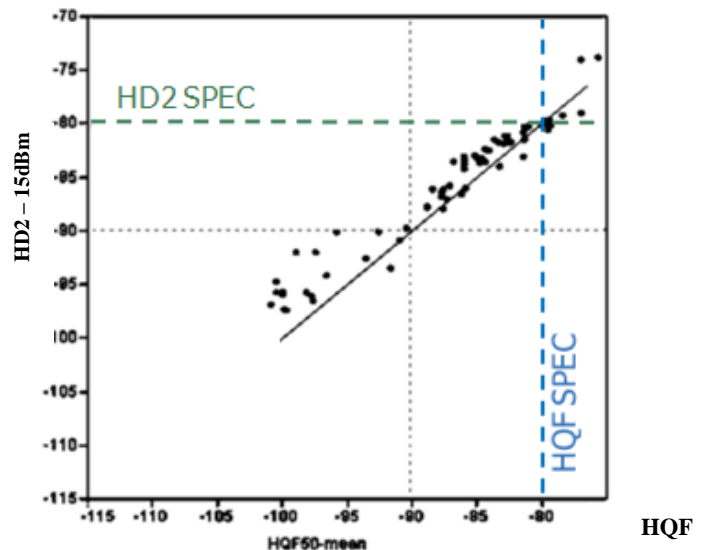


Figure 13: HD2 vs. HQF Correlation

Because there are no charge traps below the buried oxide on HR-SOI wafers, the effective resistivity at this depth is extremely low while the substrate will exhibit high resistivity when doing SRP. This explains why this methodology only works for substrates that include a trap-rich layer underneath the buried oxide.

When looking at the SRP plot (Figure 12), it is worth noting that while below a certain depth the substrate resistivity stays constant, there are some variations in and around the trap-rich layer close to the buried oxide depending on the quality of the trap-rich layer. HQF metrology takes into account this phenomenon and is much more reliable than only using the substrate resistivity as a prediction for RF performance.

Soitec has implemented this metrology on its production RFeSI SOI wafers and is sampling products to carry the HQF measurement. To address different market requirements, we set our HQF_{max} specification at -80 dBm for RFeSI80 (first-generation of Soitec RFeSI product) and at -90 dBm for our RFeSI90 (second-generation Soitec RFeSI product) (Figure 14).



Figure 14: Soitec RFeSI Products' HQF Specifications

Soitec RFeSI wafers are available in 200mm and 300mm diameter.

Conclusion

As a solution addressing the current and next generation of RF standards, Soitec RFeSI SOI wafers are enabling this market by meeting some of the most difficult LTE and LTE Advanced linearity requirements. Soitec is able to provide its customers with the RFeSI SOI substrates that meet their desired level of RF performance.

HQF metrology, conducted at the substrate level, provides a reliable measure of the finished devices' RF performance. It is now being used by Soitec to report the expected RF linearity performance of ICs manufactured with RF-SOI substrates.

About the authors

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